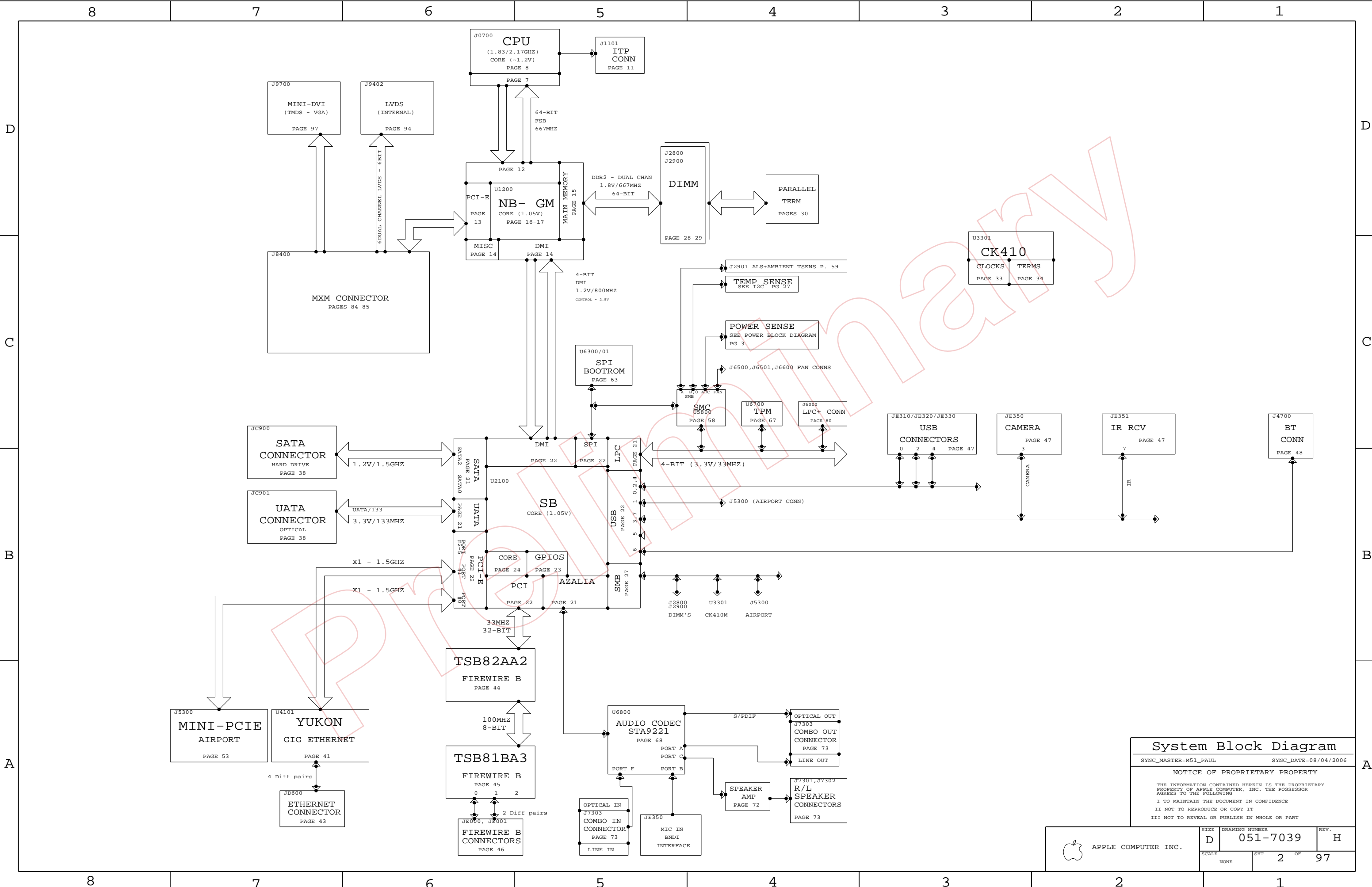


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System Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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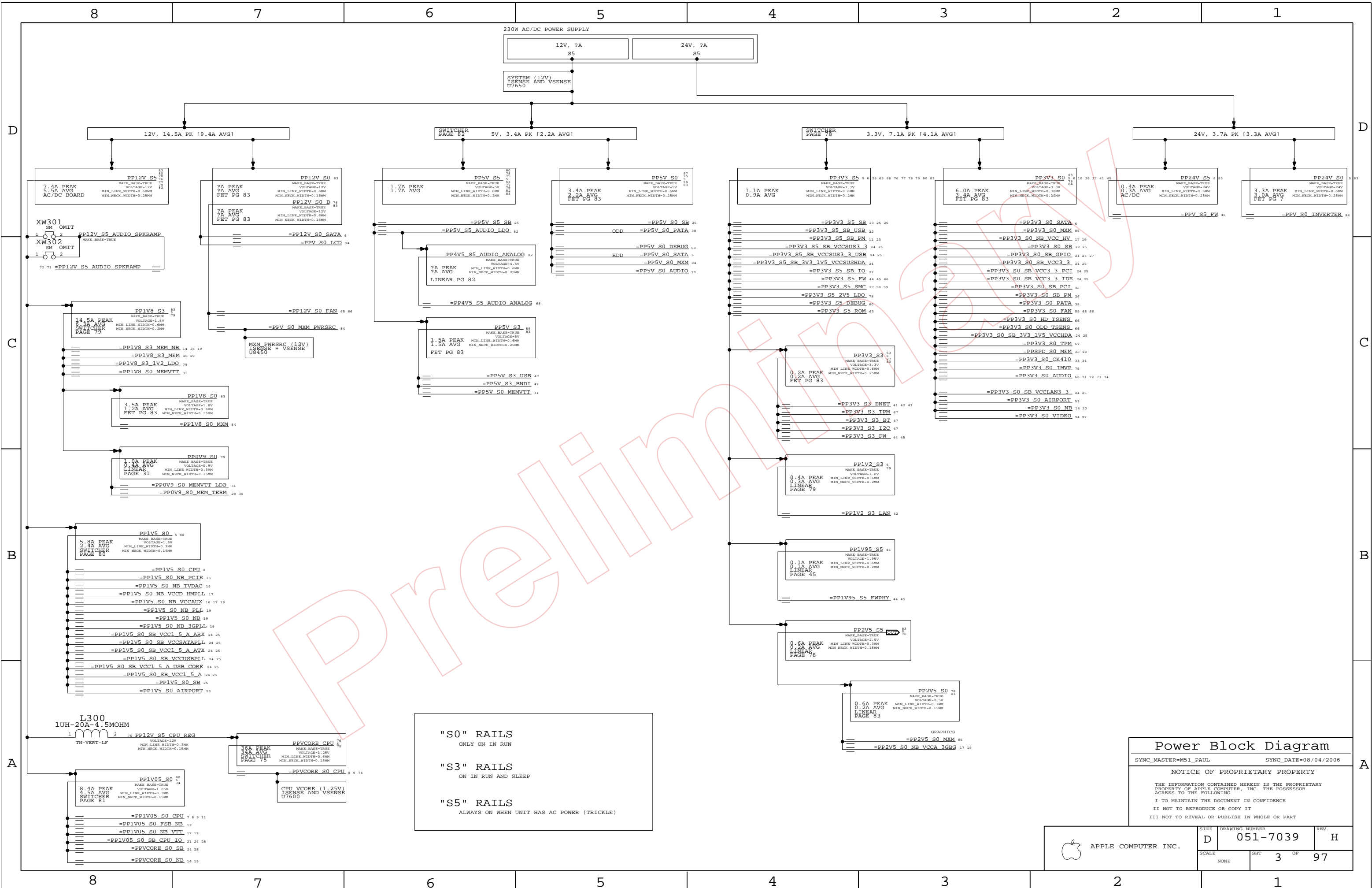
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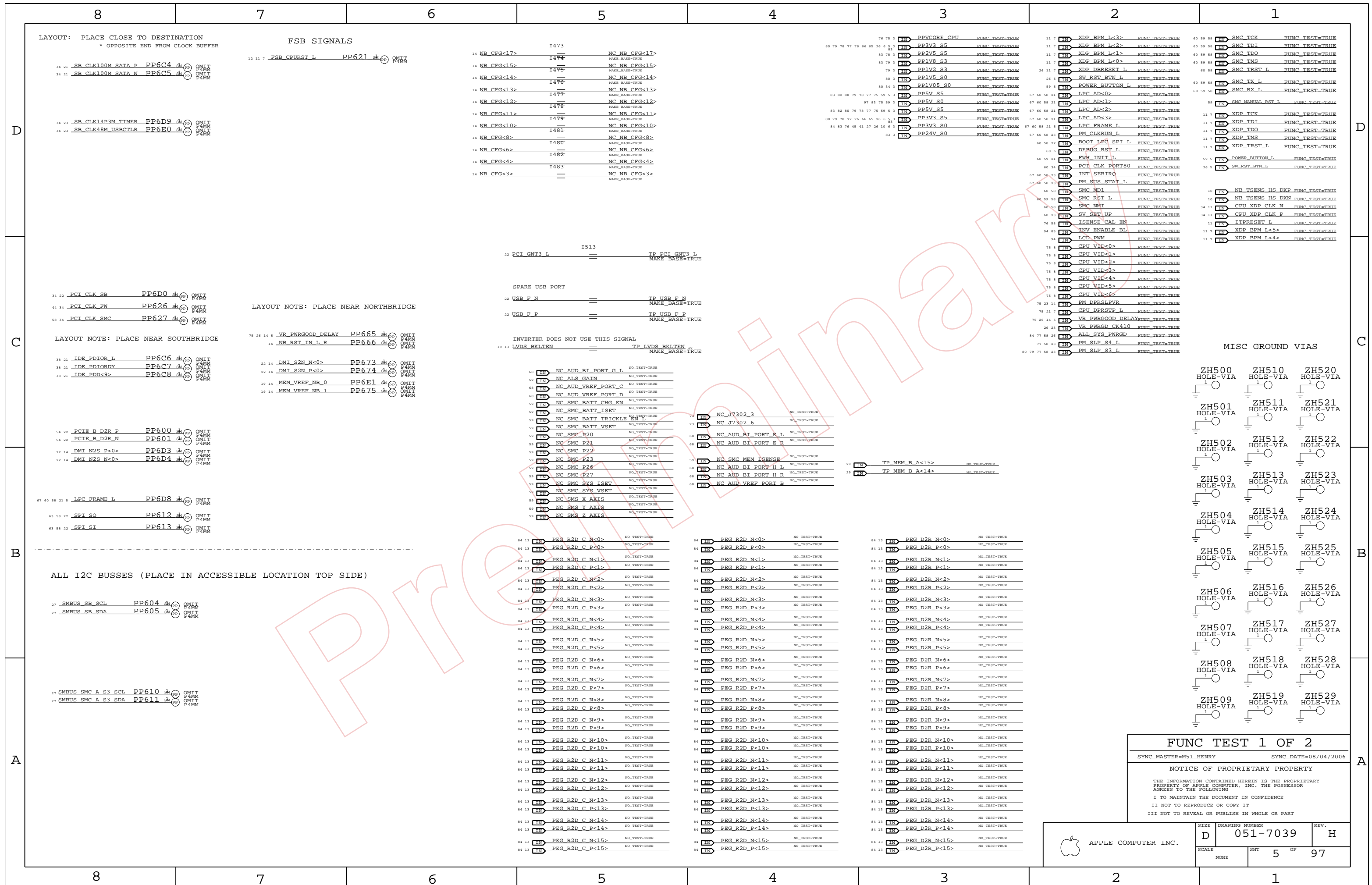
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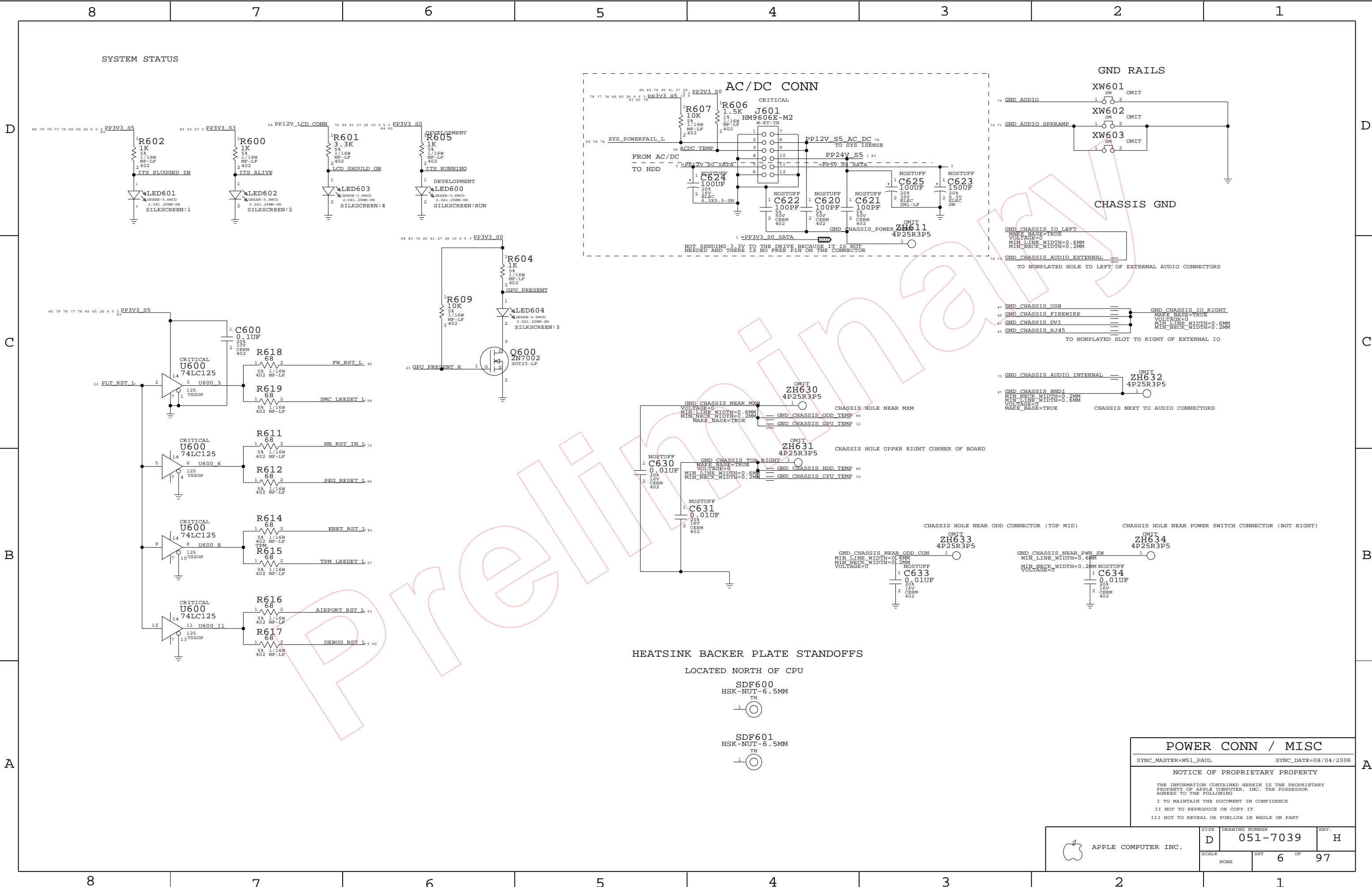
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SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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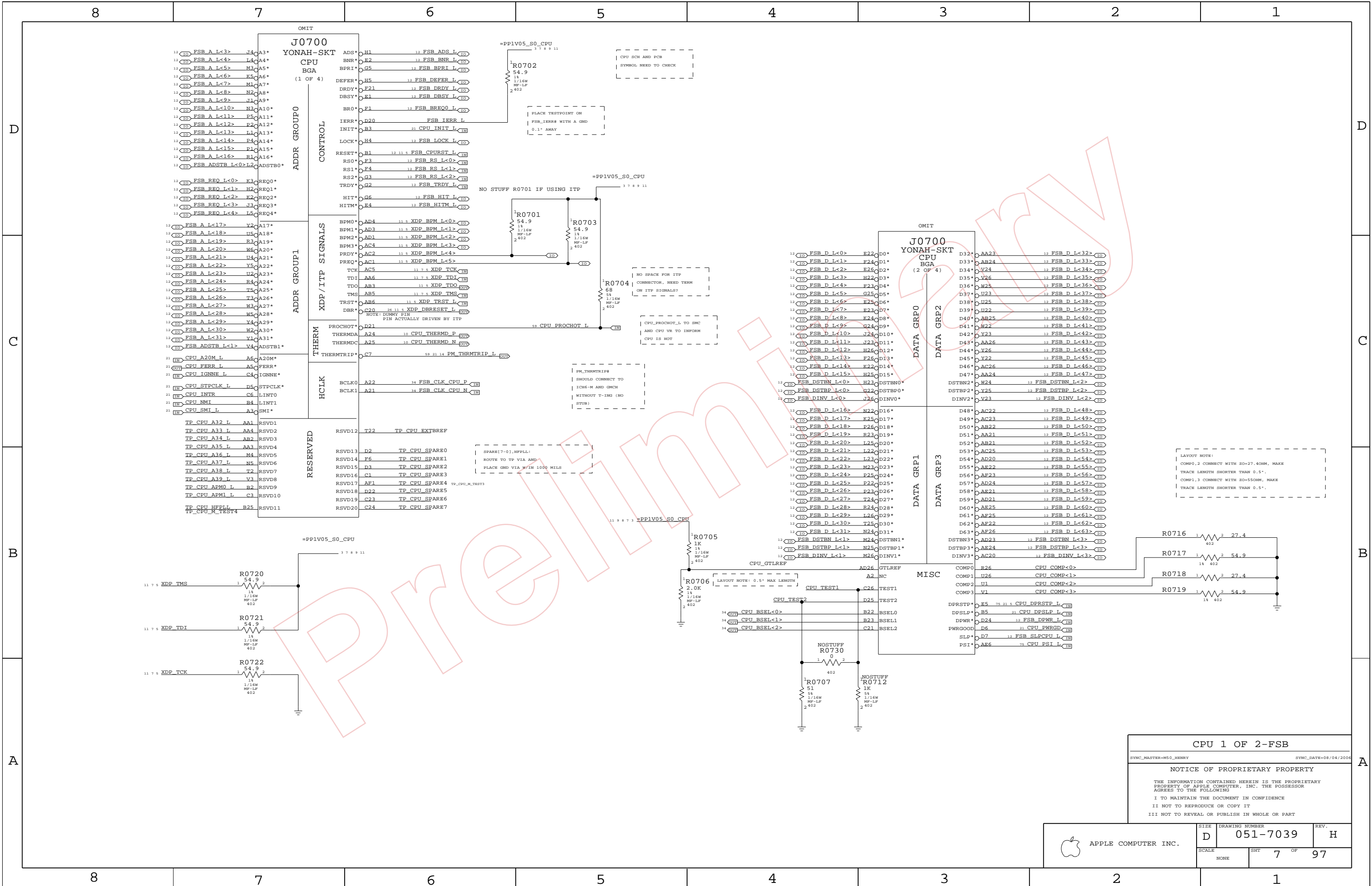
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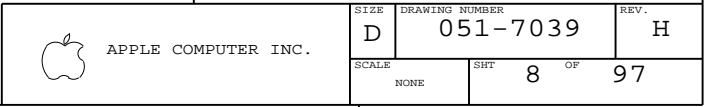
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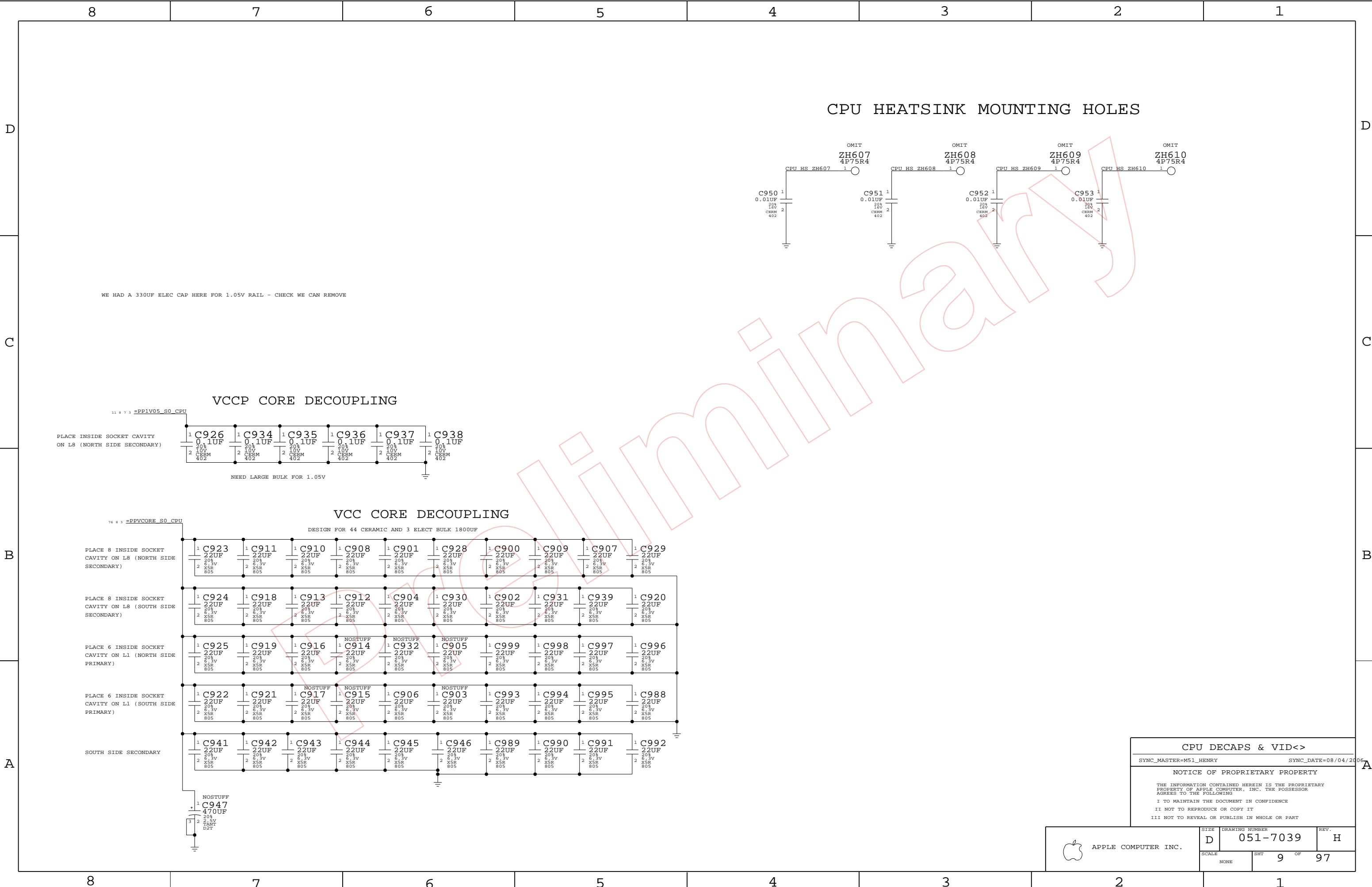
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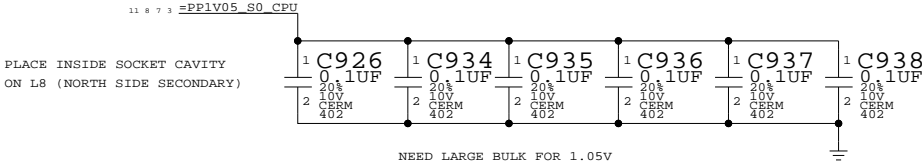




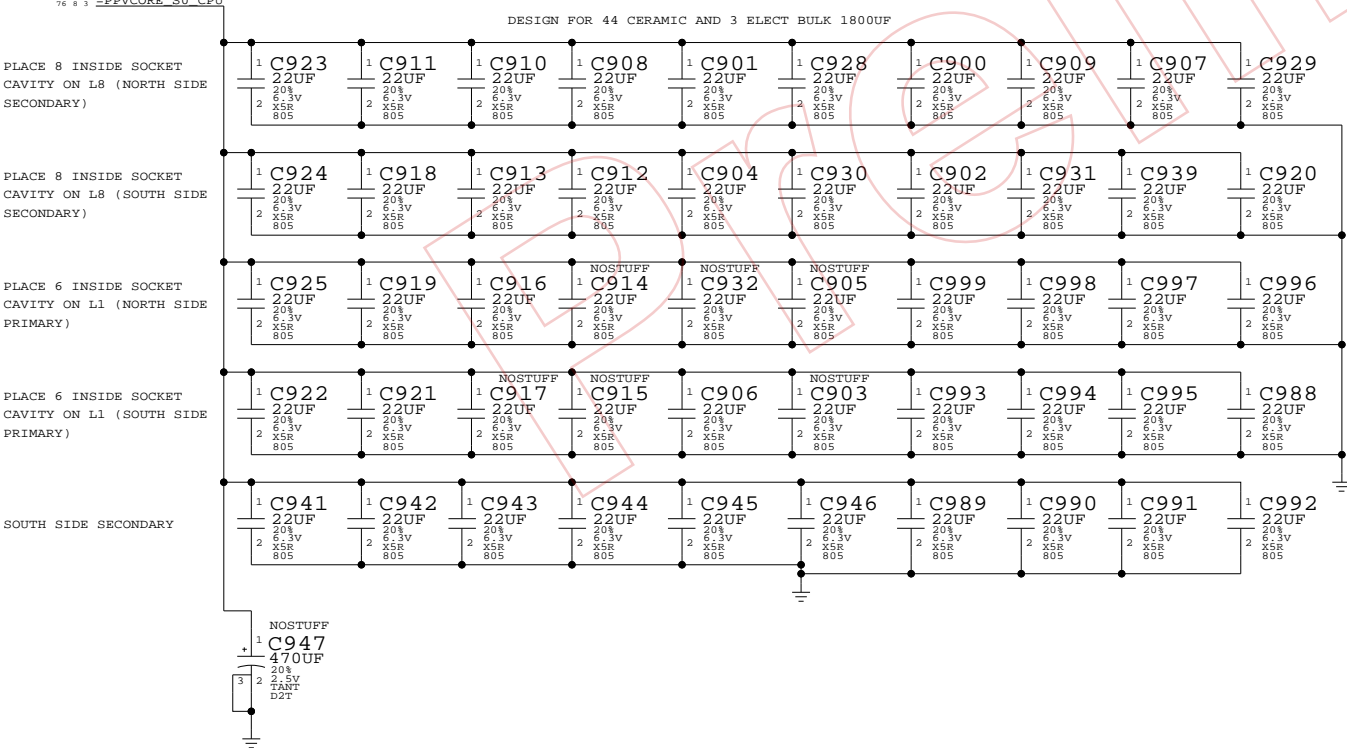


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

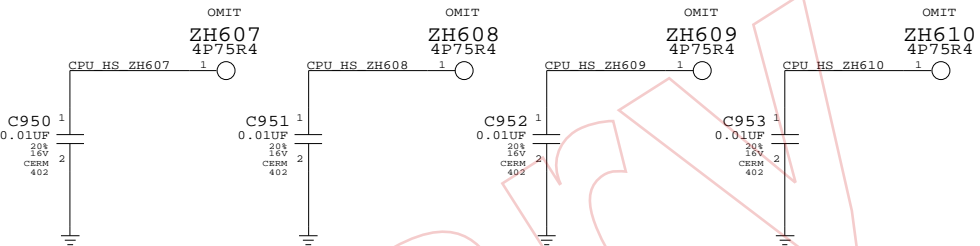
VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU HEATSINK MOUNTING HOLES



CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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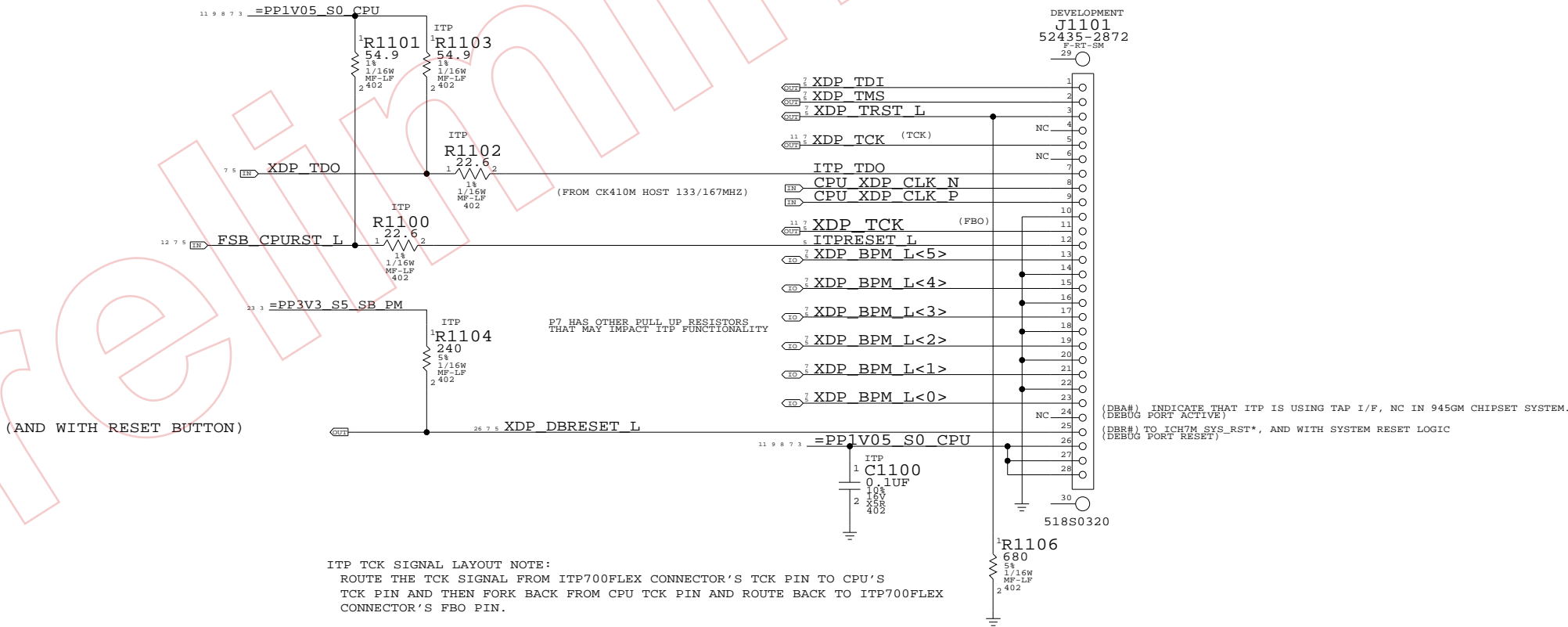
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CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	H
SCALE		SHT	11 OF 97
NONE			

D

C

B

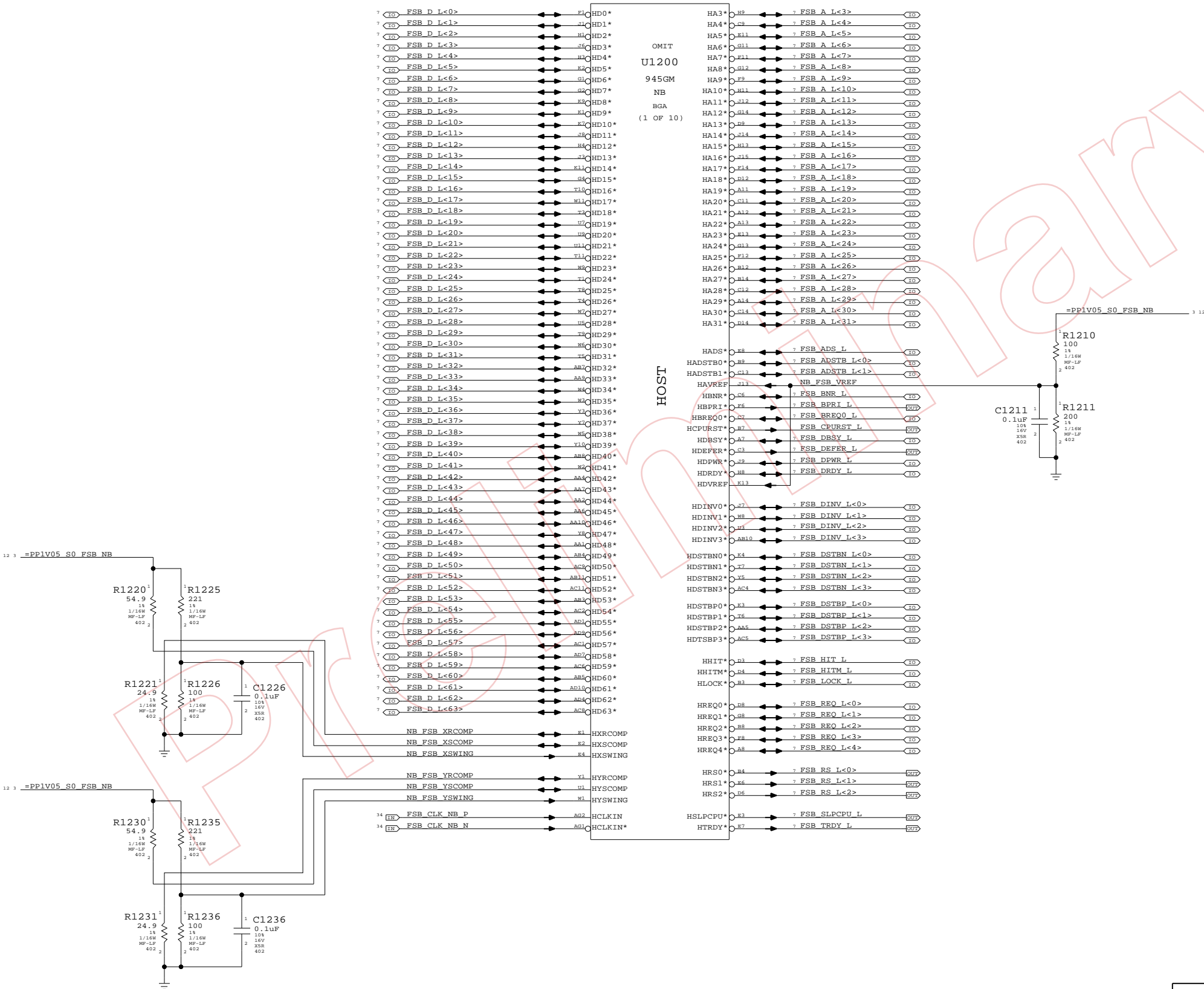
A

D

C

B

A



NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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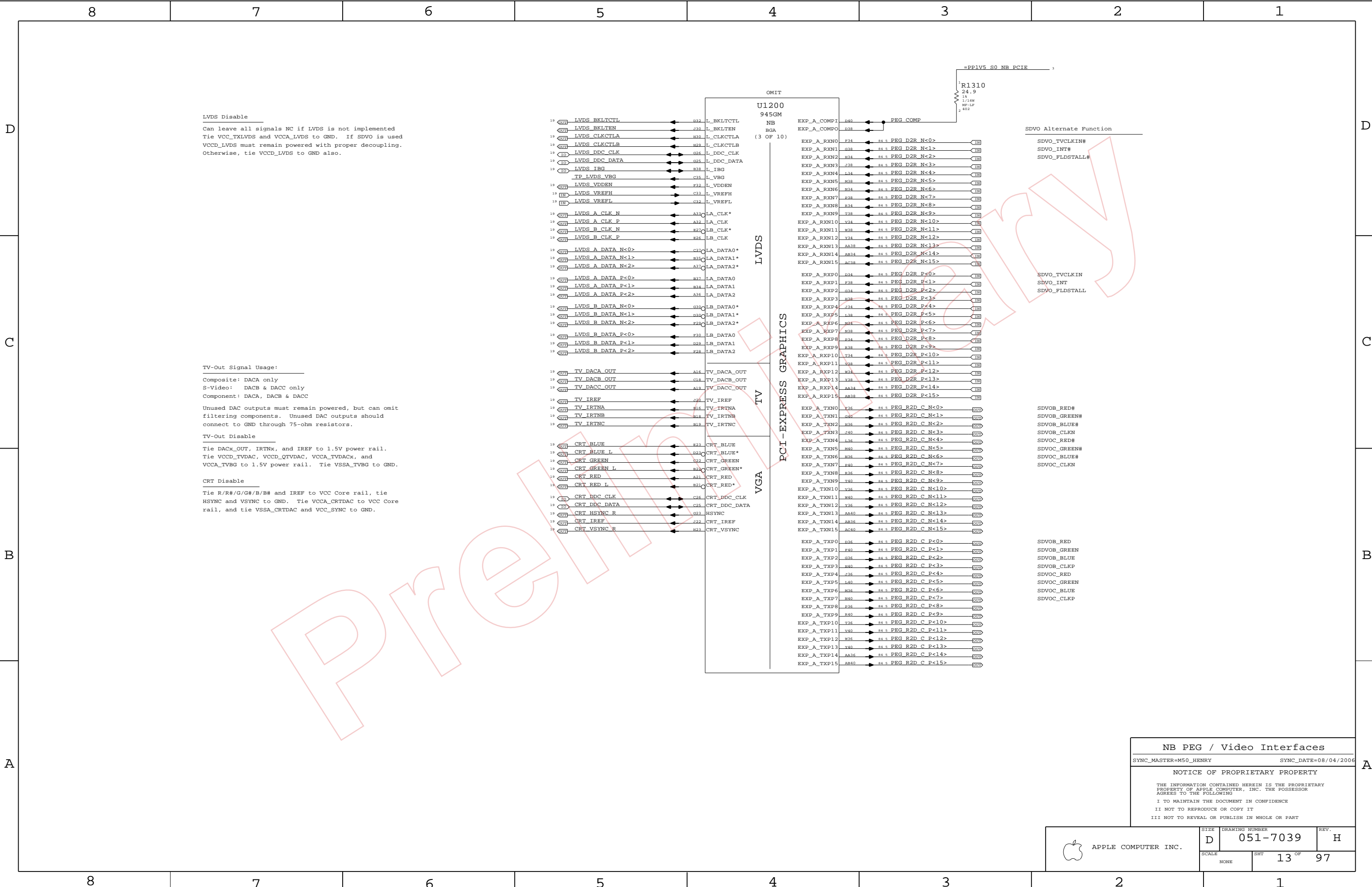
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SCALE		SHT	12 OF 97
NONE			



LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

OMIT

U1200

945GM

NB

BGA

(3 OF 10)

LVDS

TV

VGA

PCI-EXPRESS GRAPHICS

EXP_A_COMP1	D40	PEG COMP	
EXP_A_COMP0	D38		
EXP_A_RXN0	F34	PEG D2R N<0>	EXP_A_RXN0
EXP_A_RXN1	G38	PEG D2R N<1>	EXP_A_RXN1
EXP_A_RXN2	H34	PEG D2R N<2>	EXP_A_RXN2
EXP_A_RXN3	J38	PEG D2R N<3>	EXP_A_RXN3
EXP_A_RXN4	L34	PEG D2R N<4>	EXP_A_RXN4
EXP_A_RXN5	M38	PEG D2R N<5>	EXP_A_RXN5
EXP_A_RXN6	N34	PEG D2R N<6>	EXP_A_RXN6
EXP_A_RXN7	P38	PEG D2R N<7>	EXP_A_RXN7
EXP_A_RXN8	R34	PEG D2R N<8>	EXP_A_RXN8
EXP_A_RXN9	T38	PEG D2R N<9>	EXP_A_RXN9
EXP_A_RXN10	V34	PEG D2R N<10>	EXP_A_RXN10
EXP_A_RXN11	W38	PEG D2R N<11>	EXP_A_RXN11
EXP_A_RXN12	Y34	PEG D2R N<12>	EXP_A_RXN12
EXP_A_RXN13	AA38	PEG D2R N<13>	EXP_A_RXN13
EXP_A_RXN14	AB34	PEG D2R N<14>	EXP_A_RXN14
EXP_A_RXN15	AC38	PEG D2R N<15>	EXP_A_RXN15
EXP_A_RXP0	D34	PEG D2R P<0>	EXP_A_RXP0
EXP_A_RXP1	F38	PEG D2R P<1>	EXP_A_RXP1
EXP_A_RXP2	G34	PEG D2R P<2>	EXP_A_RXP2
EXP_A_RXP3	H38	PEG D2R P<3>	EXP_A_RXP3
EXP_A_RXP4	J34	PEG D2R P<4>	EXP_A_RXP4
EXP_A_RXP5	L38	PEG D2R P<5>	EXP_A_RXP5
EXP_A_RXP6	M34	PEG D2R P<6>	EXP_A_RXP6
EXP_A_RXP7	N38	PEG D2R P<7>	EXP_A_RXP7
EXP_A_RXP8	P34	PEG D2R P<8>	EXP_A_RXP8
EXP_A_RXP9	R38	PEG D2R P<9>	EXP_A_RXP9
EXP_A_RXP10	T34	PEG D2R P<10>	EXP_A_RXP10
EXP_A_RXP11	V38	PEG D2R P<11>	EXP_A_RXP11
EXP_A_RXP12	W34	PEG D2R P<12>	EXP_A_RXP12
EXP_A_RXP13	Y38	PEG D2R P<13>	EXP_A_RXP13
EXP_A_RXP14	AA34	PEG D2R P<14>	EXP_A_RXP14
EXP_A_RXP15	AB38	PEG D2R P<15>	EXP_A_RXP15
EXP_A_TXN0	F36	PEG R2D C N<0>	EXP_A_TXN0
EXP_A_TXN1	G40	PEG R2D C N<1>	EXP_A_TXN1
EXP_A_TXN2	H36	PEG R2D C N<2>	EXP_A_TXN2
EXP_A_TXN3	J40	PEG R2D C N<3>	EXP_A_TXN3
EXP_A_TXN4	L36	PEG R2D C N<4>	EXP_A_TXN4
EXP_A_TXN5	M40	PEG R2D C N<5>	EXP_A_TXN5
EXP_A_TXN6	N36	PEG R2D C N<6>	EXP_A_TXN6
EXP_A_TXN7	P40	PEG R2D C N<7>	EXP_A_TXN7
EXP_A_TXN8	R36	PEG R2D C N<8>	EXP_A_TXN8
EXP_A_TXN9	T40	PEG R2D C N<9>	EXP_A_TXN9
EXP_A_TXN10	V36	PEG R2D C N<10>	EXP_A_TXN10
EXP_A_TXN11	W40	PEG R2D C N<11>	EXP_A_TXN11
EXP_A_TXN12	Y36	PEG R2D C N<12>	EXP_A_TXN12
EXP_A_TXN13	AA40	PEG R2D C N<13>	EXP_A_TXN13
EXP_A_TXN14	AB36	PEG R2D C N<14>	EXP_A_TXN14
EXP_A_TXN15	AC40	PEG R2D C N<15>	EXP_A_TXN15
EXP_A_TXP0	D36	PEG R2D C P<0>	EXP_A_TXP0
EXP_A_TXP1	F40	PEG R2D C P<1>	EXP_A_TXP1
EXP_A_TXP2	G36	PEG R2D C P<2>	EXP_A_TXP2
EXP_A_TXP3	H40	PEG R2D C P<3>	EXP_A_TXP3
EXP_A_TXP4	J36	PEG R2D C P<4>	EXP_A_TXP4
EXP_A_TXP5	L40	PEG R2D C P<5>	EXP_A_TXP5
EXP_A_TXP6	M36	PEG R2D C P<6>	EXP_A_TXP6
EXP_A_TXP7	N40	PEG R2D C P<7>	EXP_A_TXP7
EXP_A_TXP8	P36	PEG R2D C P<8>	EXP_A_TXP8
EXP_A_TXP9	R40	PEG R2D C P<9>	EXP_A_TXP9
EXP_A_TXP10	T36	PEG R2D C P<10>	EXP_A_TXP10
EXP_A_TXP11	V40	PEG R2D C P<11>	EXP_A_TXP11
EXP_A_TXP12	W36	PEG R2D C P<12>	EXP_A_TXP12
EXP_A_TXP13	Y40	PEG R2D C P<13>	EXP_A_TXP13
EXP_A_TXP14	AA36	PEG R2D C P<14>	EXP_A_TXP14
EXP_A_TXP15	AB40	PEG R2D C P<15>	EXP_A_TXP15

SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY

SYNC_DATE=08/04/2006

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SIZE

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DRAWING NUMBER

051-7039

REV.

H

SCALE

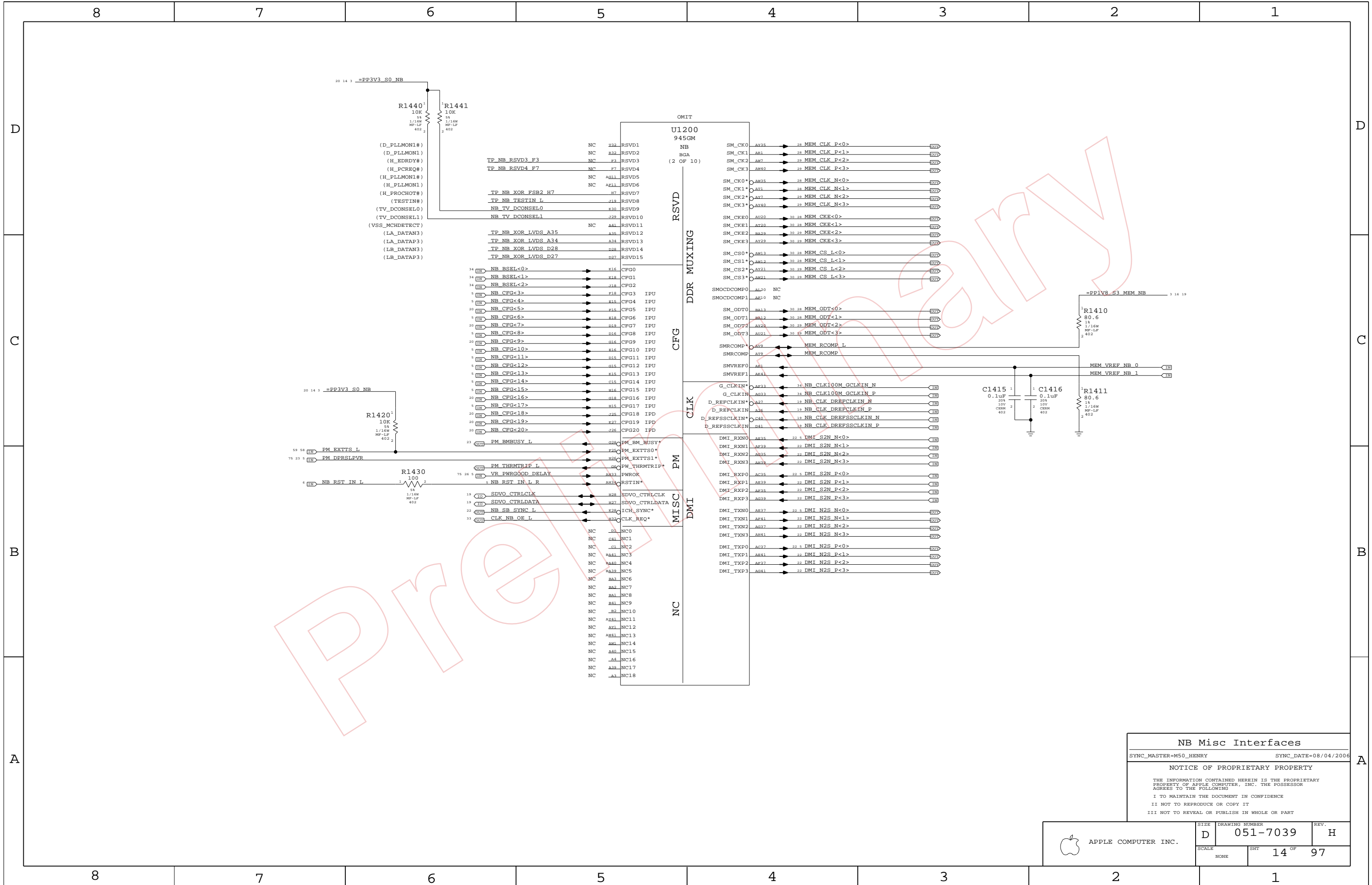
NONE

SHT

13

OF

97



NB Misc Interfaces

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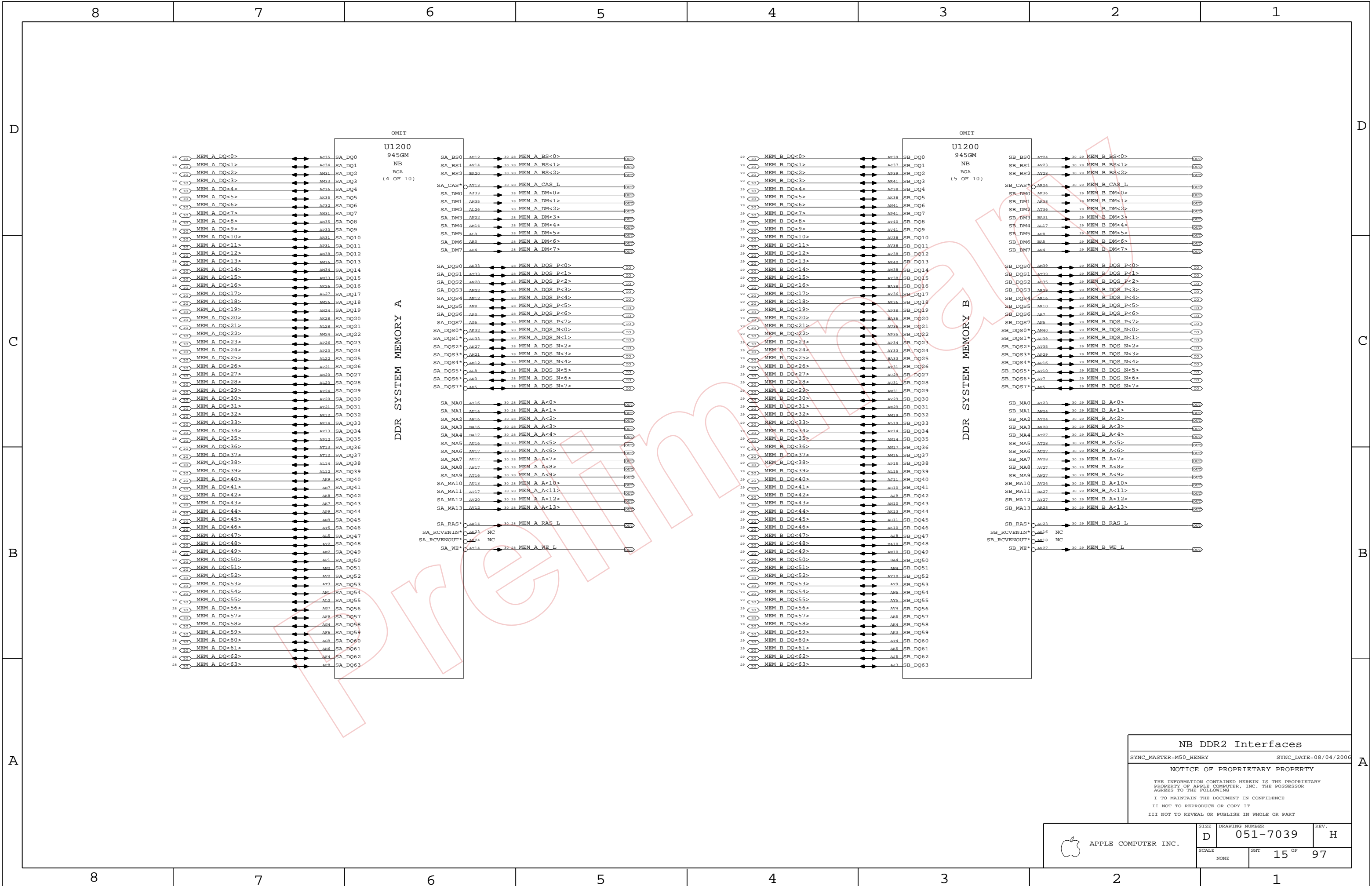
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7039 REV. H

SCALE NONE SHT 14 OF 97



NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

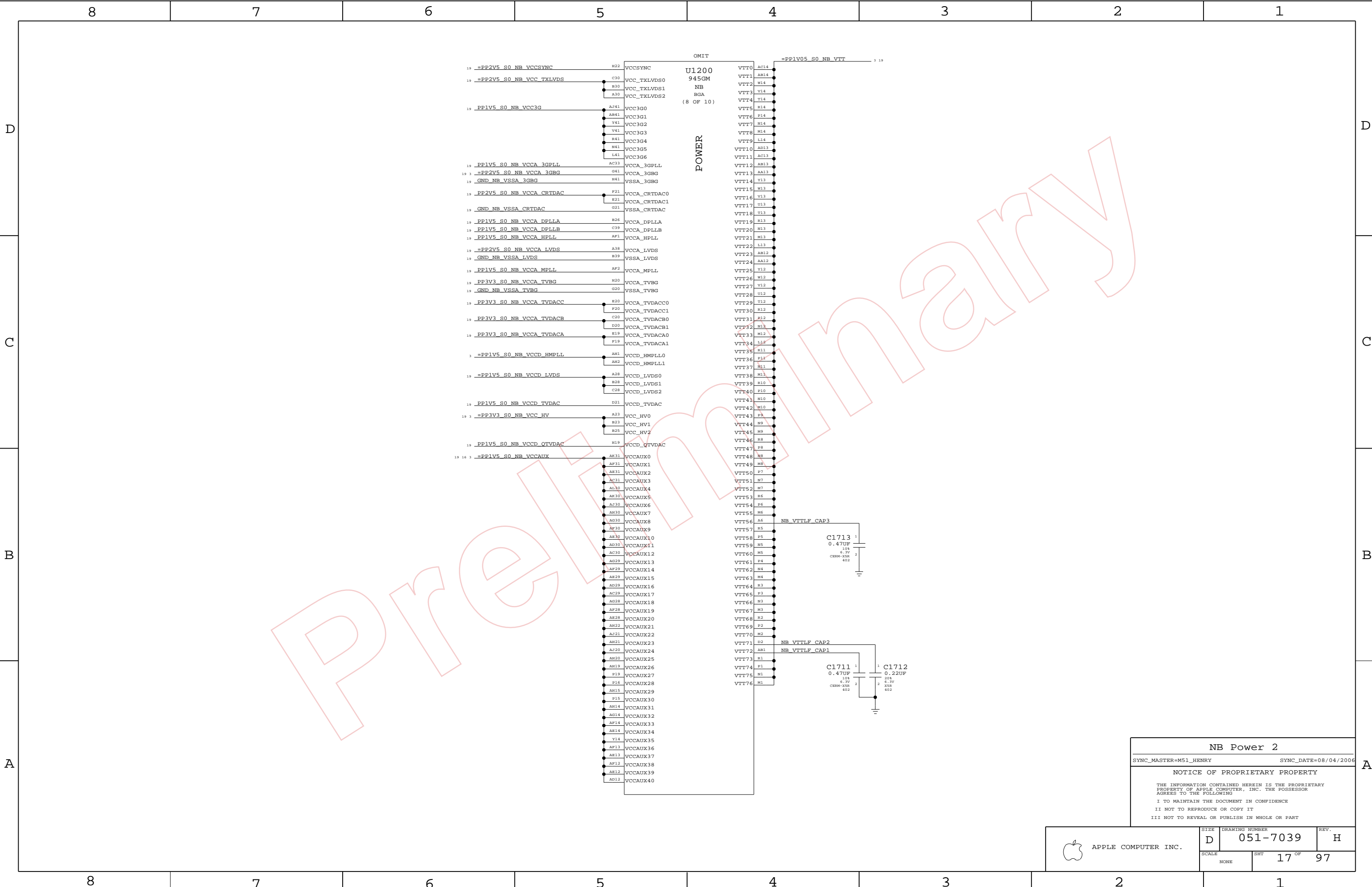
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NB Power 2

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7039

REV.

H

SCALE

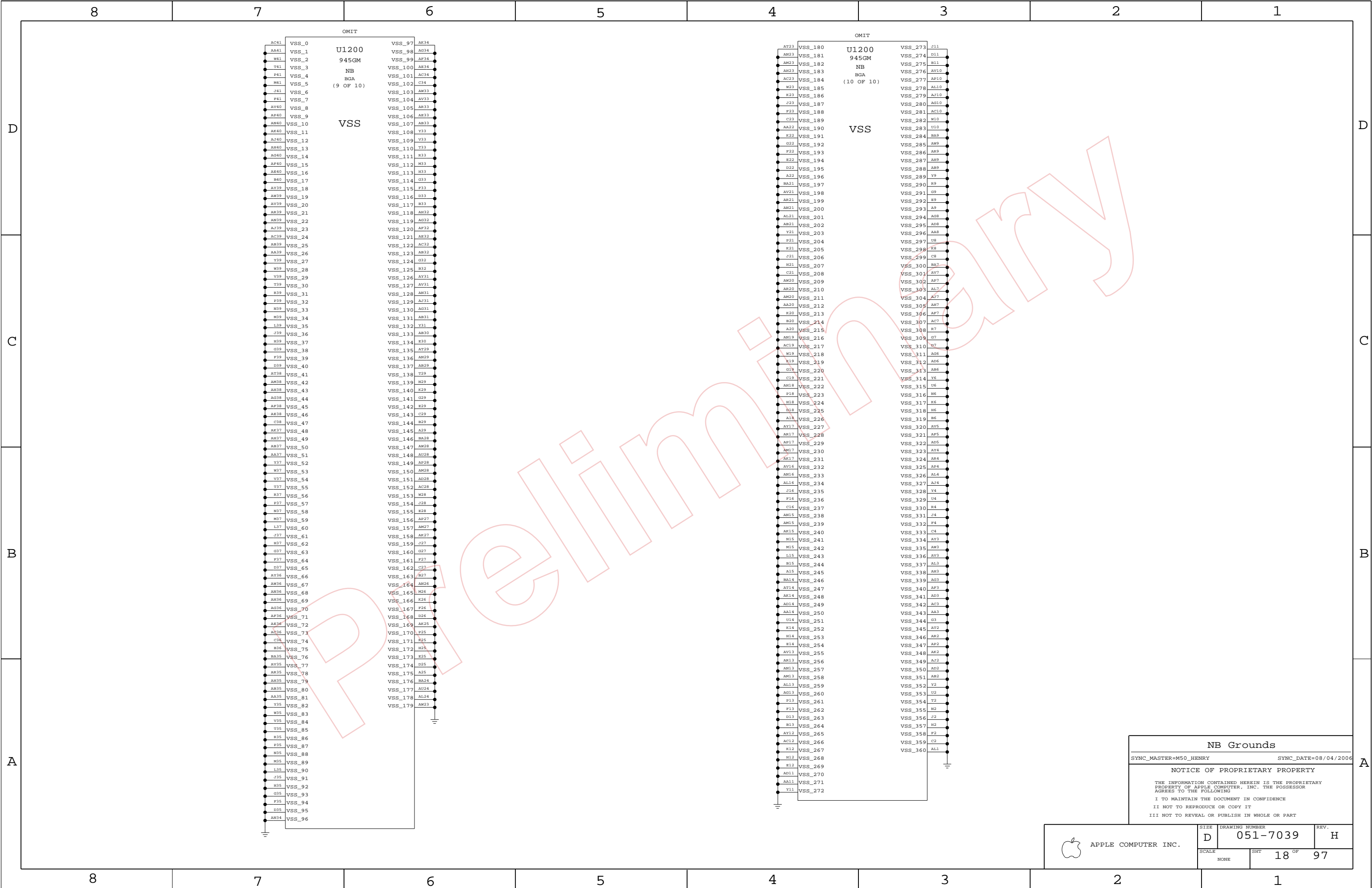
NONE

SHT

17

OF

97



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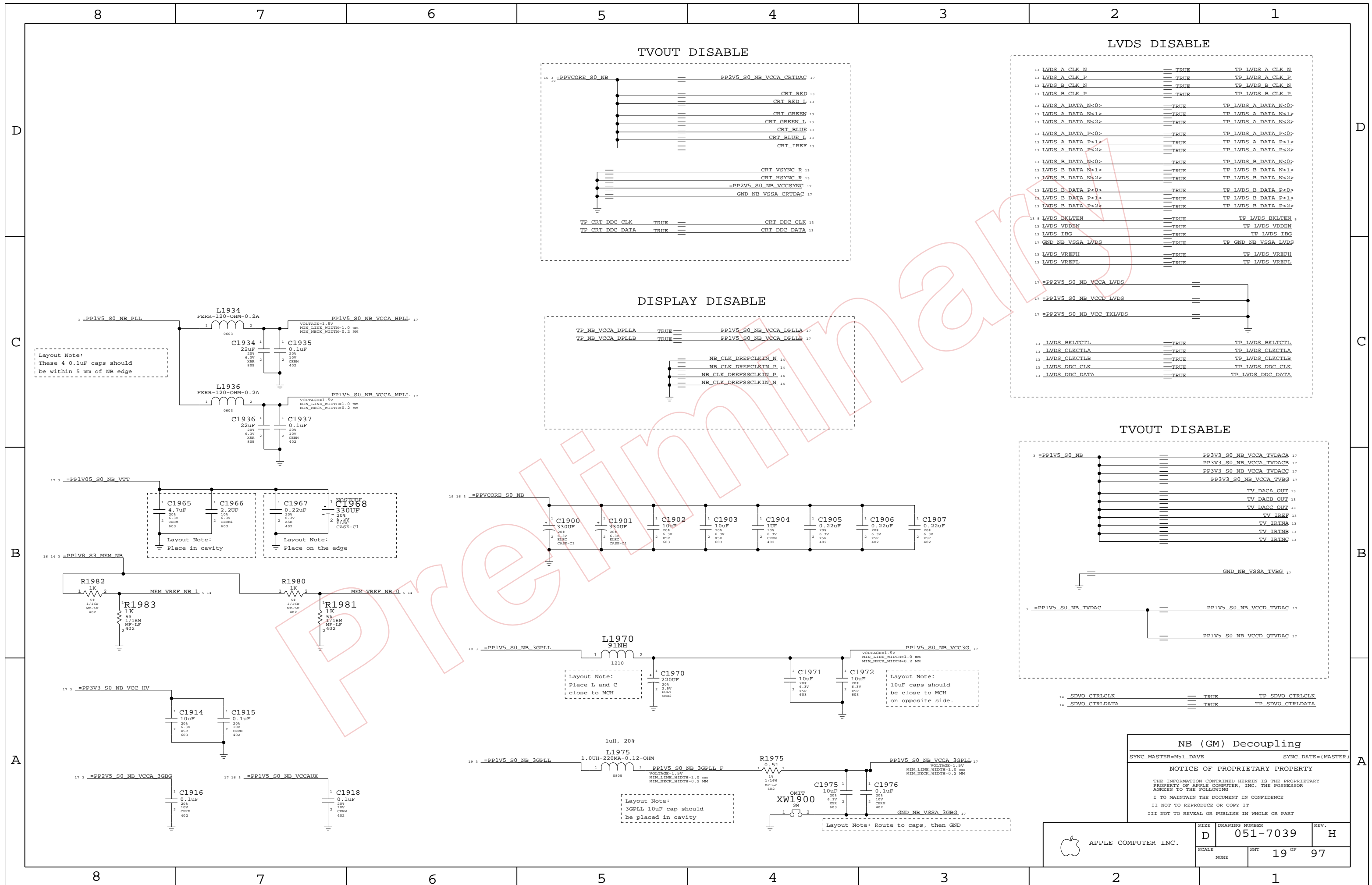
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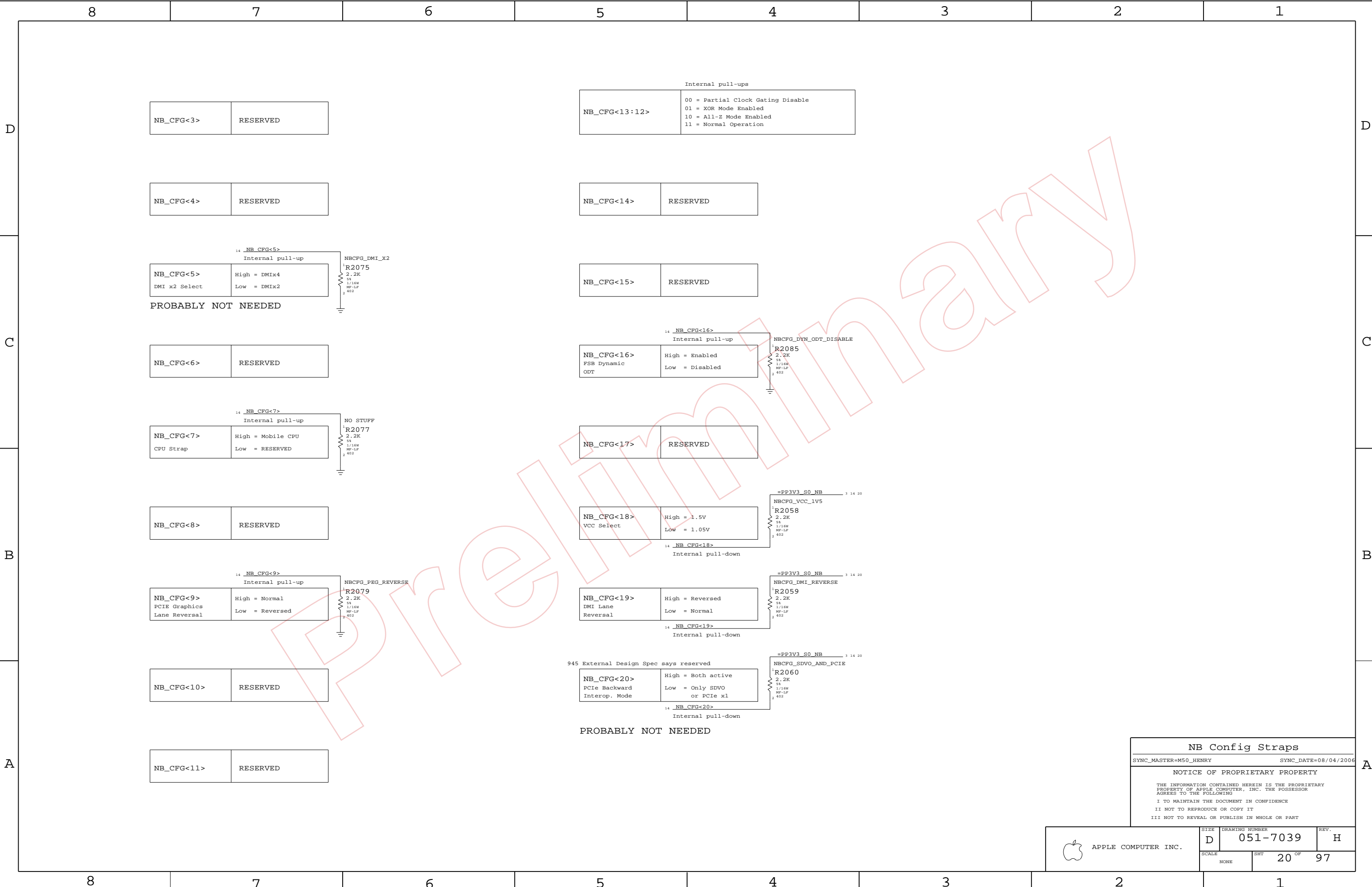
D

C

B

A





NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

NOTICE OF PROPRIETARY PROPERTY

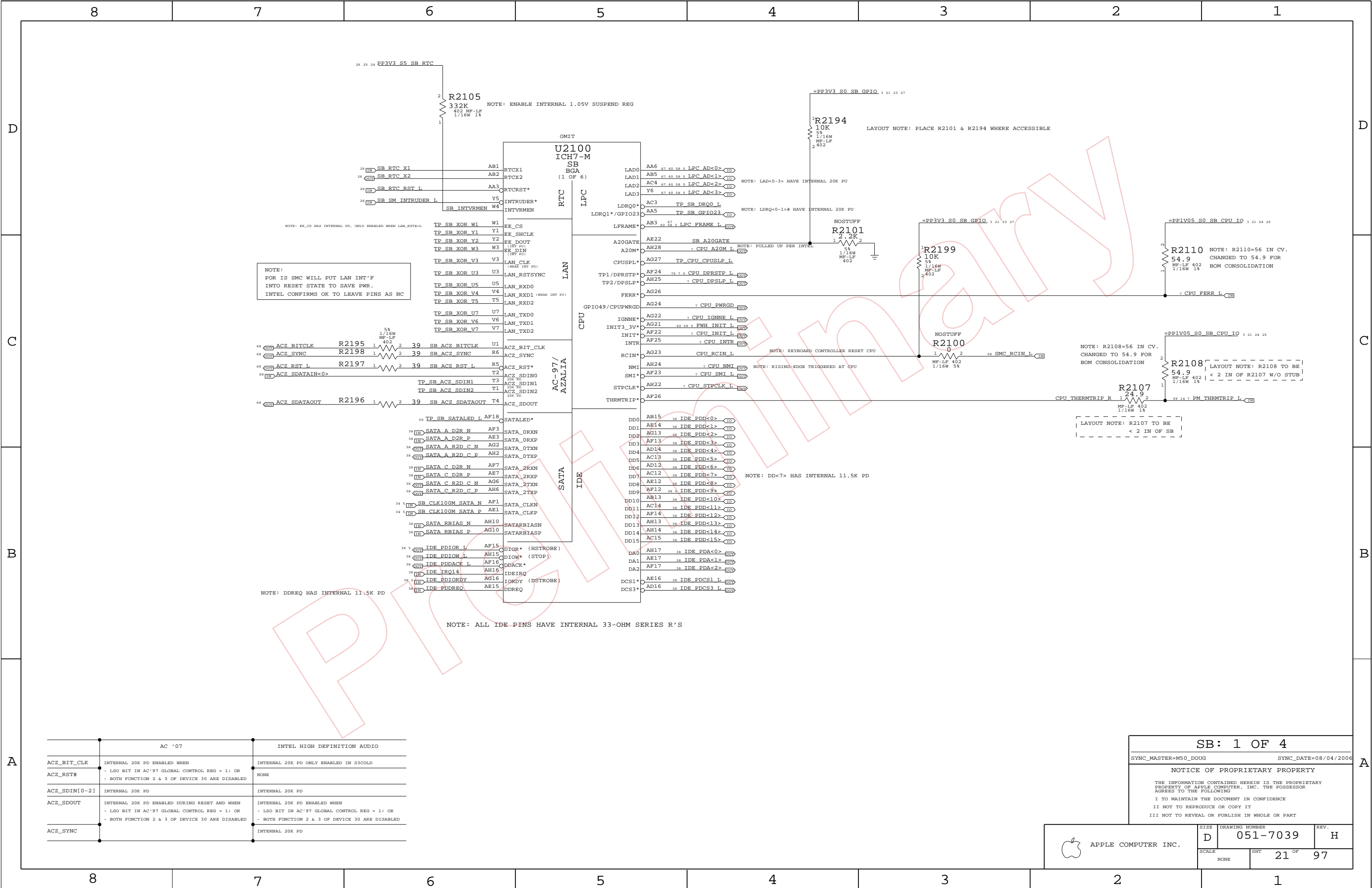
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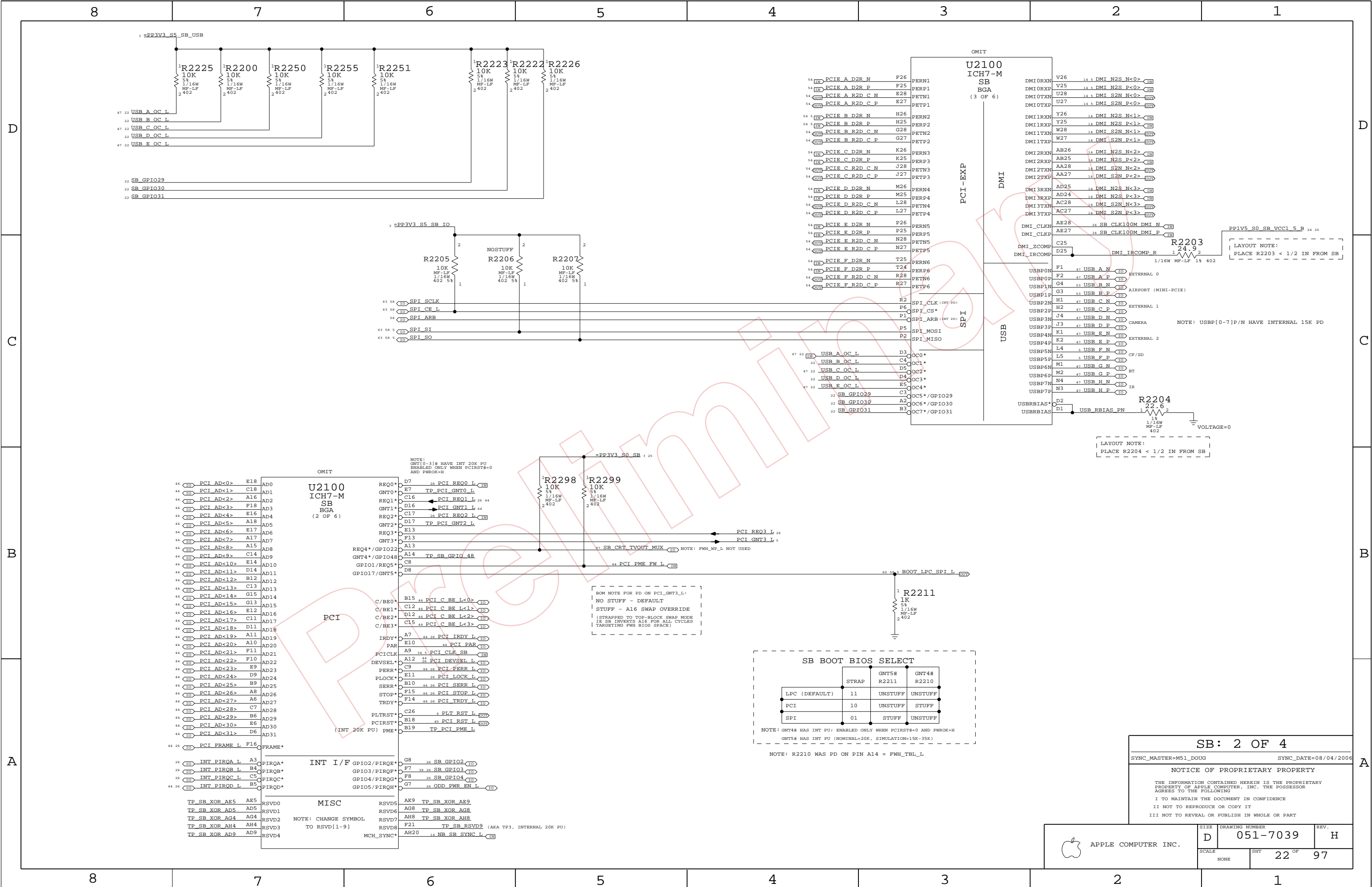
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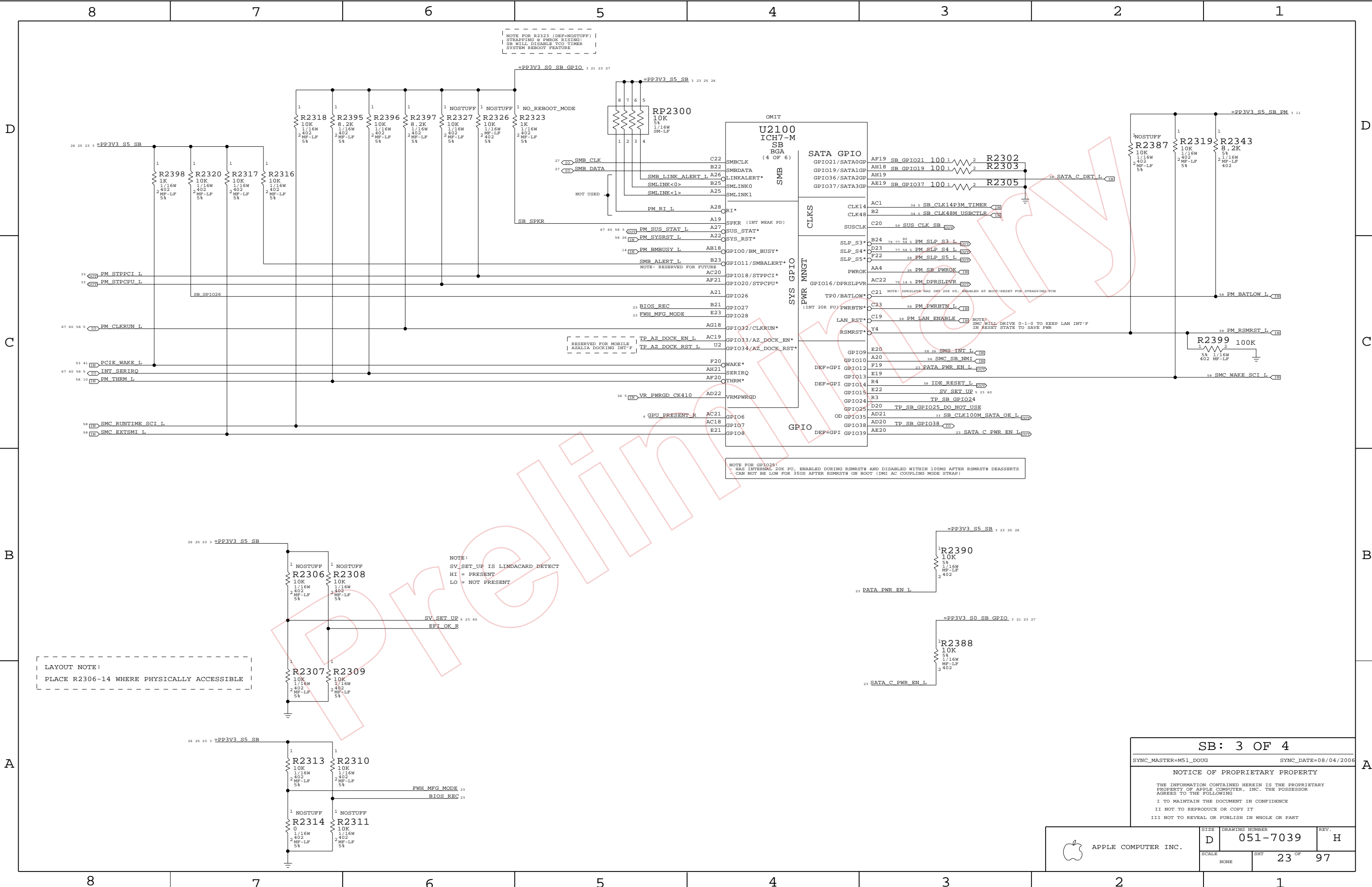
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. H
	SCALE NONE	SHT 20 OF 97	





SB: 2 OF 4		
SYNC_MASTER=M51_D0UG		SYNC_DATE=08/04/2006
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	D	051-7039	H
SCALE		SHT	22 OF 97
NONE			

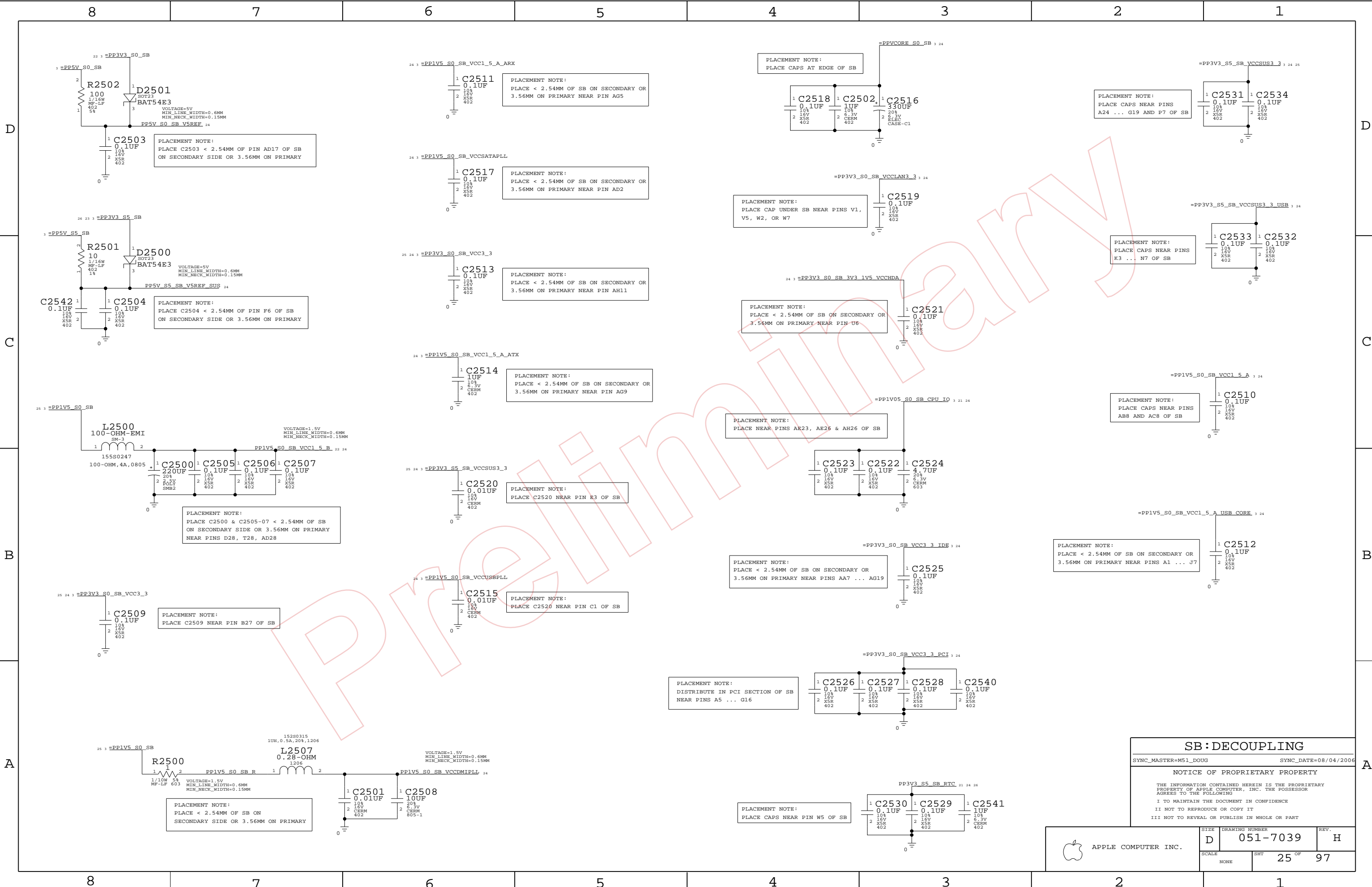


NOTE FOR R2323 (DEF-NOSTUFF) |
STRAPPING & PWROK RISING |
SB WILL DISABLE TCO TIMER |
SYSTEM REBOOT FEATURE |

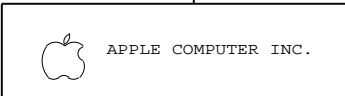
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

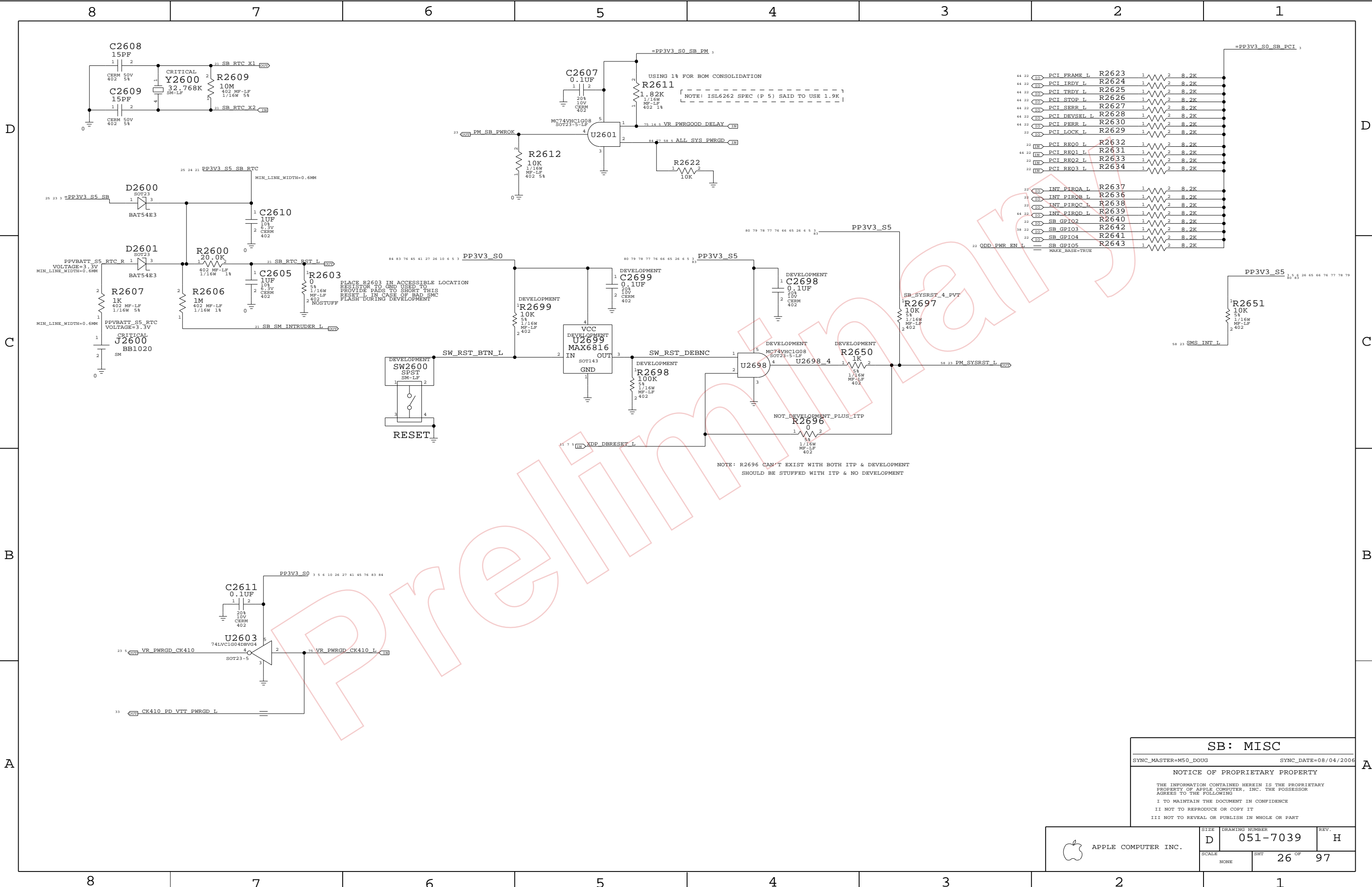
LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
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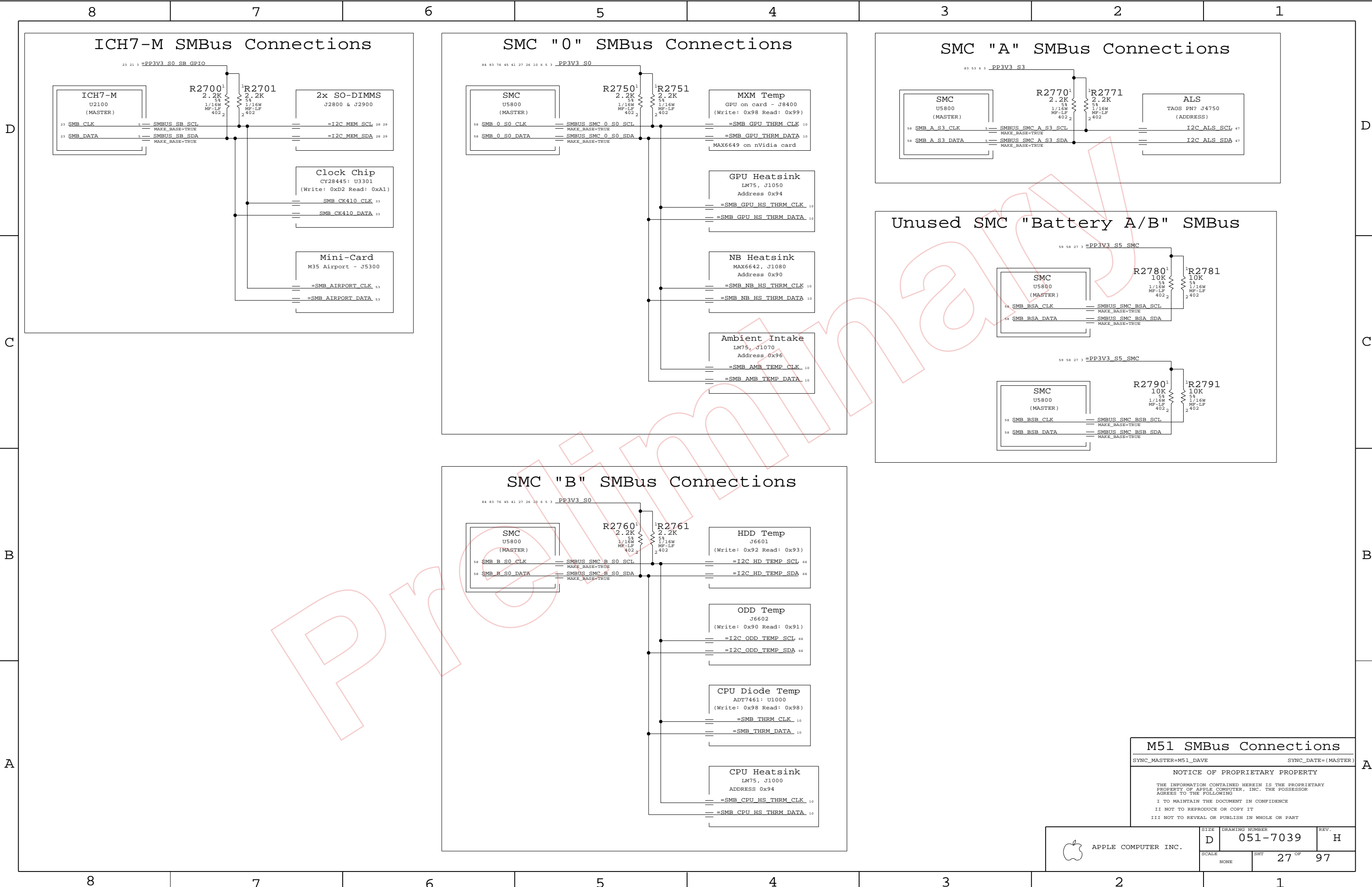
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SYNC_MASTER=M51_D0UG		SYNC_DATE=08/04/2006
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NONE		





SB: MISC	
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. H
	SCALE NONE	SHT 26 OF 97	



Page Notes

Power aliases required by this page:

- =P1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

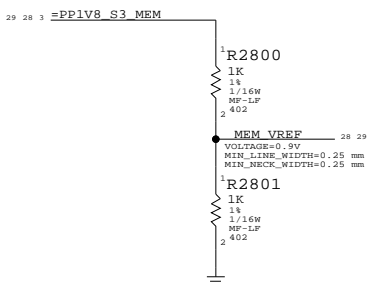
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:

(NONE)

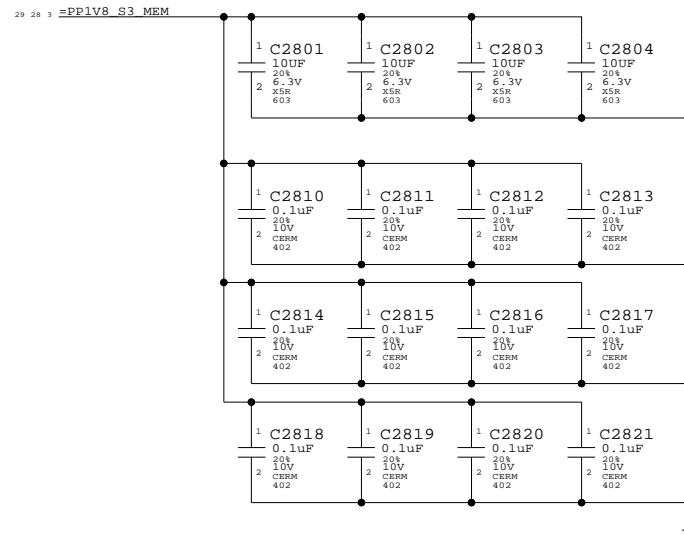
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M51 HENRY SYNC_DATE=08/04/2006

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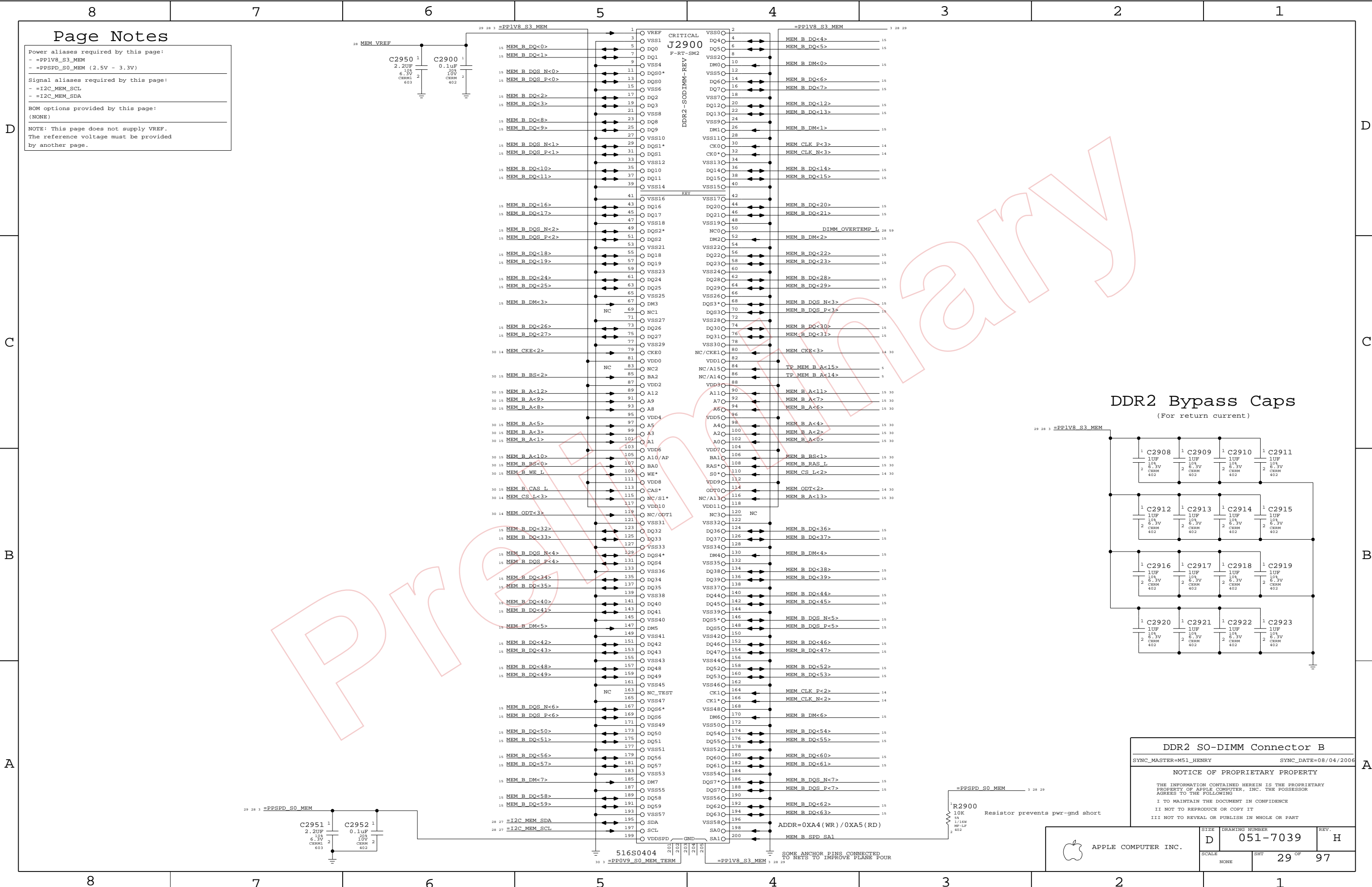
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7039 REV. H

SCALE NONE SHT 28 OF 97



Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

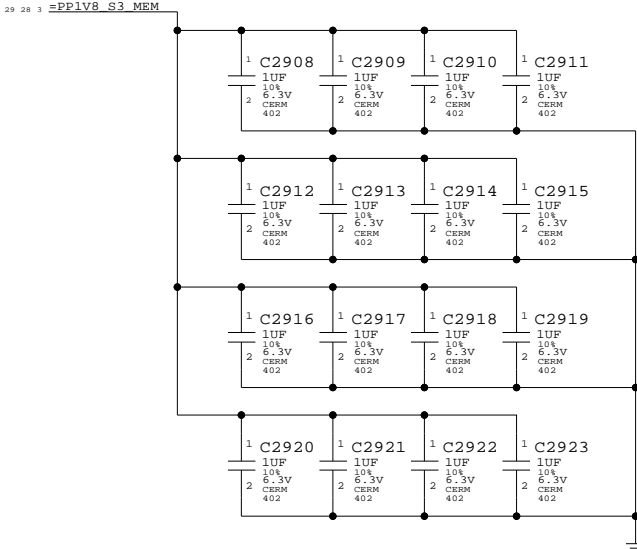
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY

SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

SIZE D

DRAWING NUMBER 051-7039

REV. H

SCALE NONE

SHT 29

OF 97

=PPSPD_S0_MEM

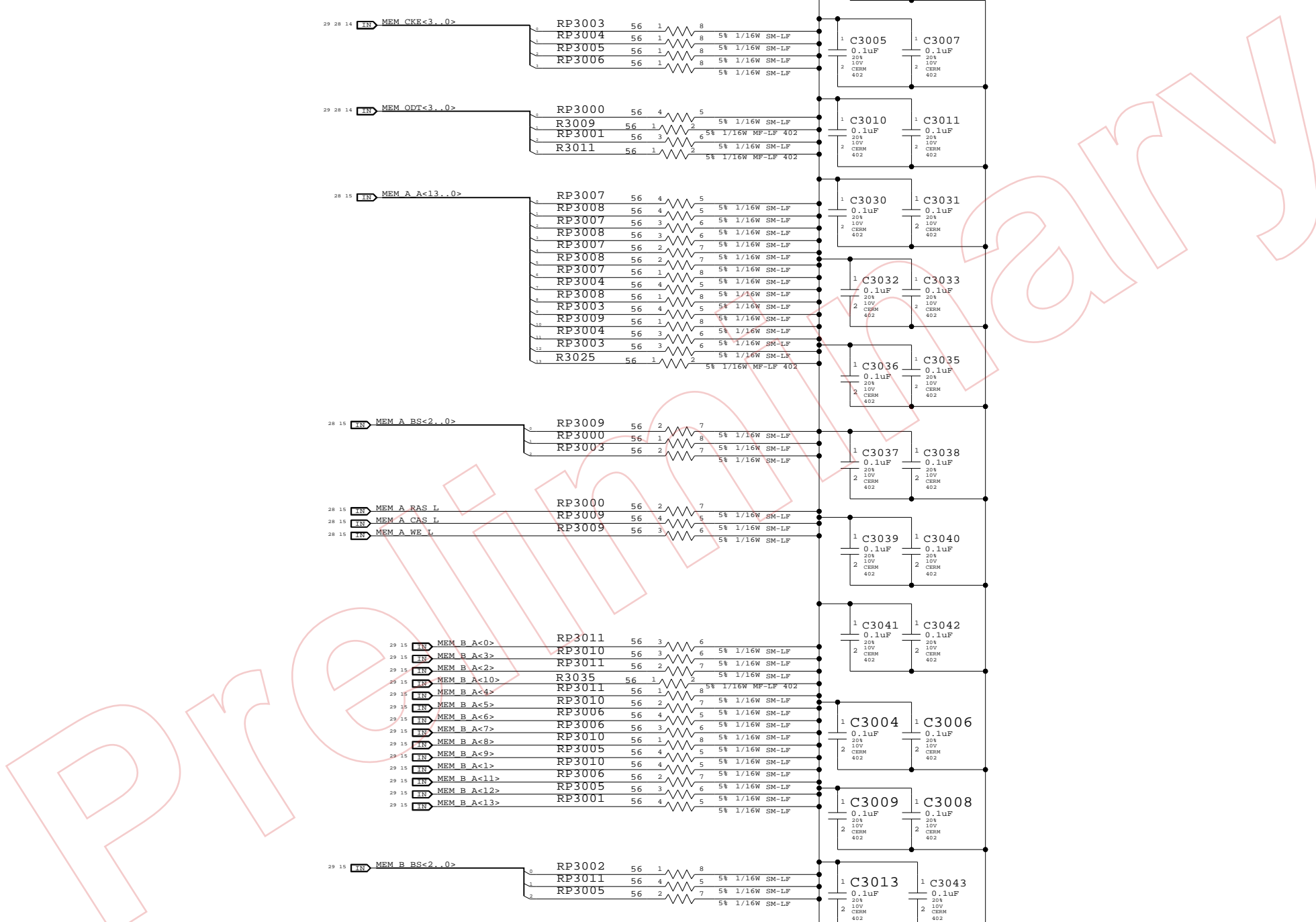
1R2900

10K

5% 1/16W NF-1P

Resistor prevents pwr-gnd short

SOME ANCHOR PINS CONNECTED TO NETS TO IMPROVE PLANE POUR



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SIZE D	DRAWING NUMBER 051-7039	REV. H
SCALE NONE	SHT 30	OF 97

```
Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PPlV8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO
```

```
Signal aliases required by this page:
(NONE)
```

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BOM options provided by this page:
(NONE)
```

[illegible]

SYNC_MASTER=M50_HENRY	SYNC_DATE=08/04/2006
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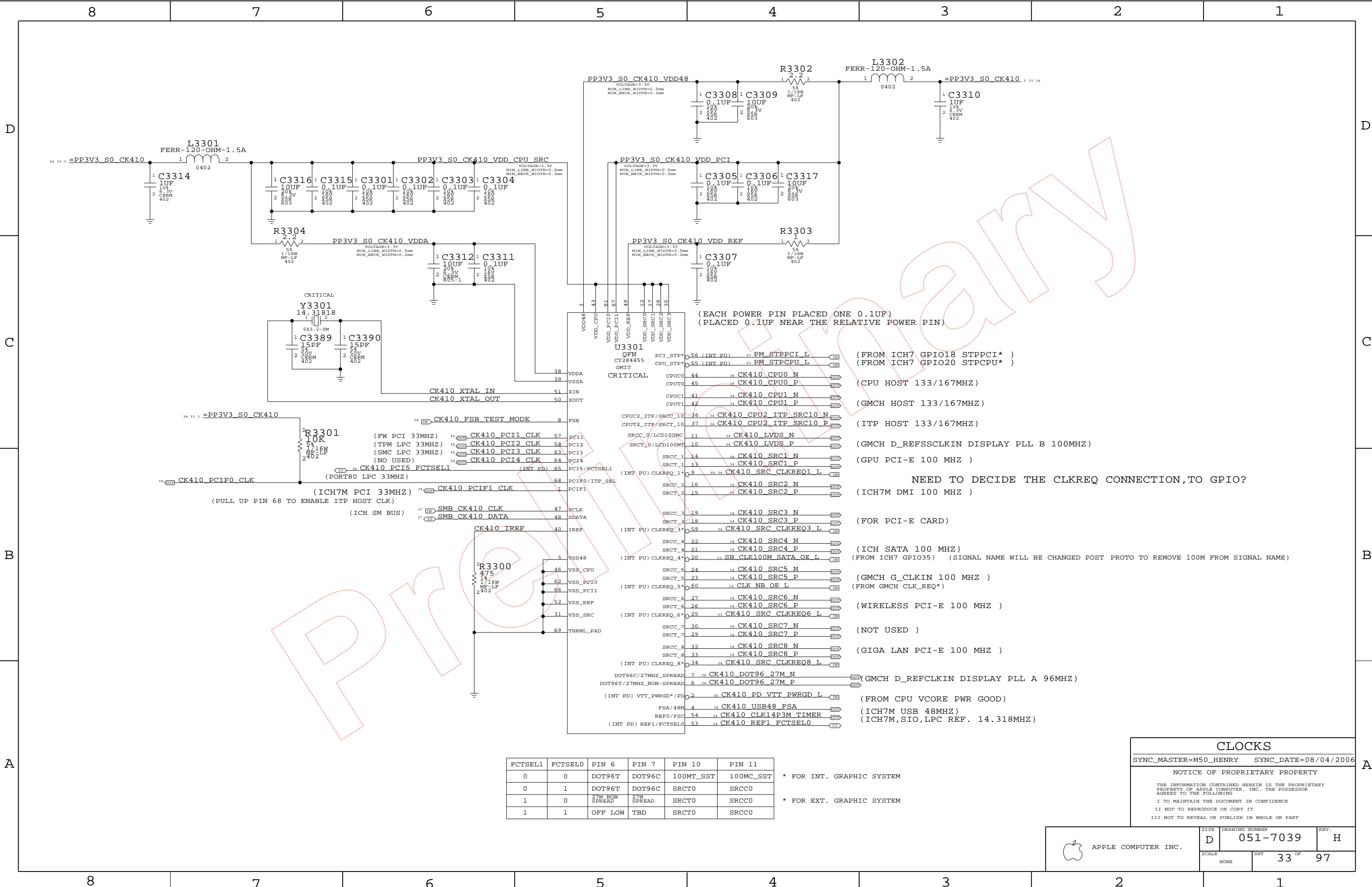


SIZE	DRAWING NUMBER	REV.
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D	051-7039
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CODE	DATE OF	

SCALE	SHI	31	OF	97
NONE				



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION,TO GPIO?
(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)
(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G_CLKIN 100 MHZ)
(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)
(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

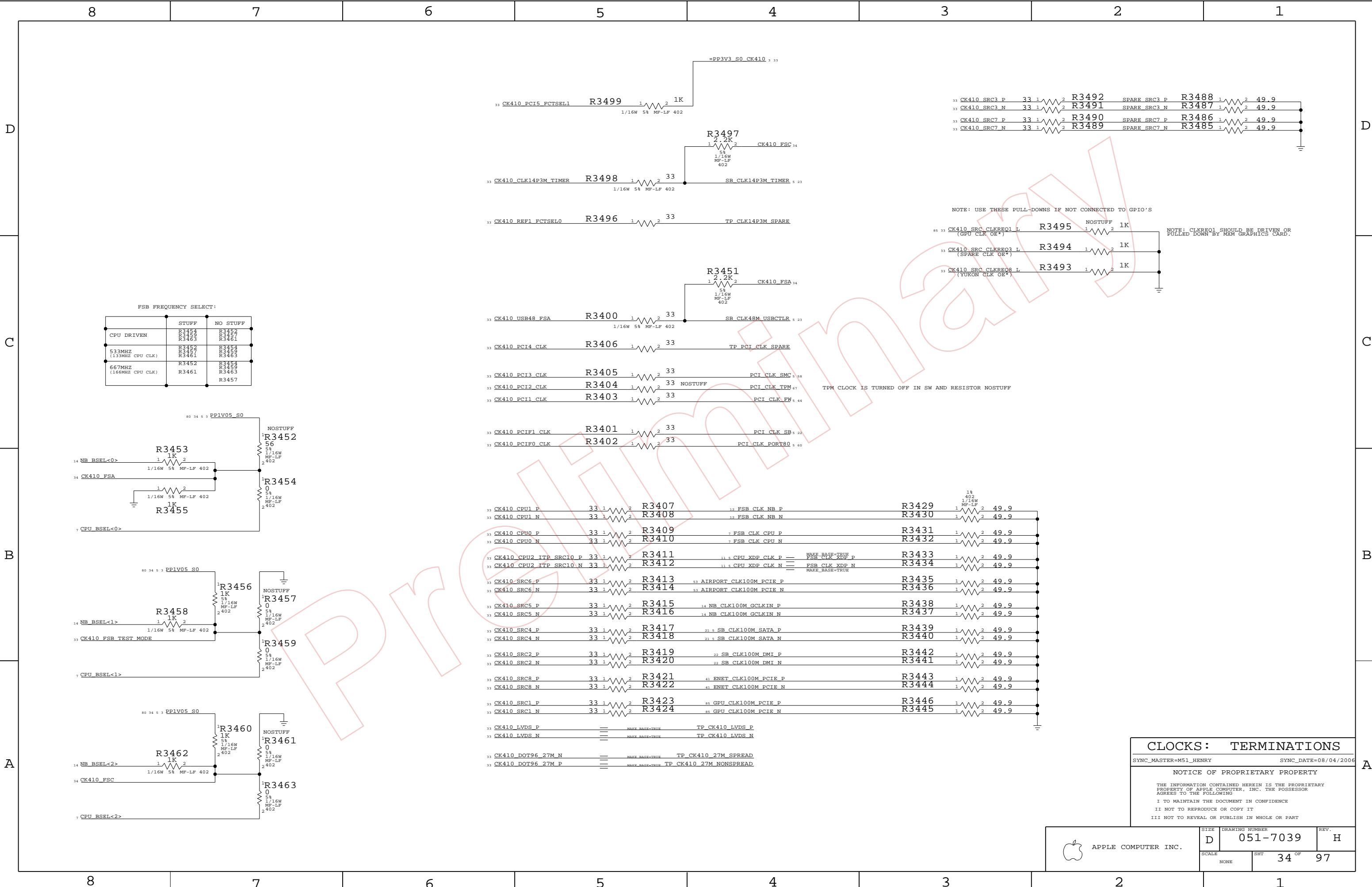
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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE	SHT	33 OF 97
NONE		



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3455 R3461	R3452 R3453 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3457	R3454 R3455 R3461
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3457	R3454 R3455 R3461

CLOCKS: TERMINATIONS

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SCALE	NONE	SHT	34 OF 97		

D

C

B

A

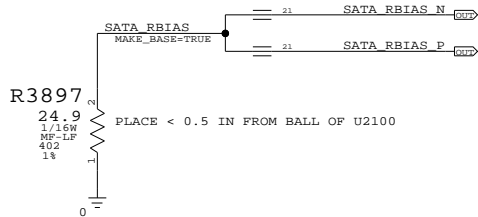
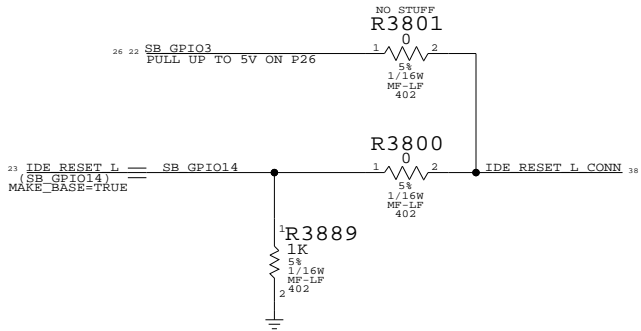
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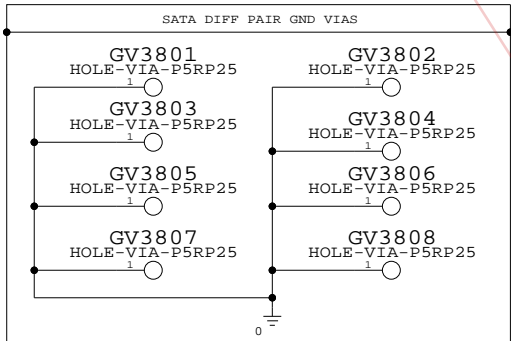
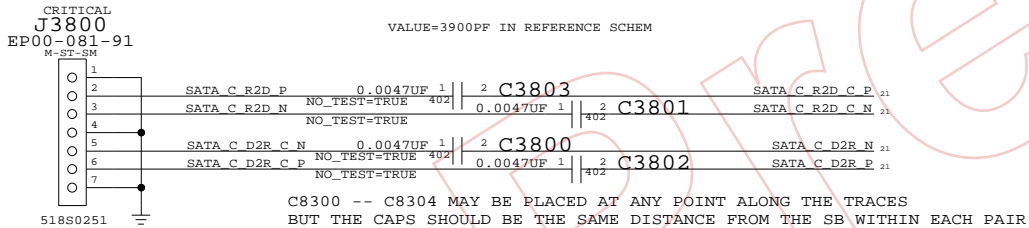
B

A

PATA (ODD) CONNECTOR



SATA CONNECTOR



SATA PORT 0 IS NOT USED

SATA A R2D C P

TP_SATA A R2D P

MAKE_BASE=TRUE

SATA A R2D C N

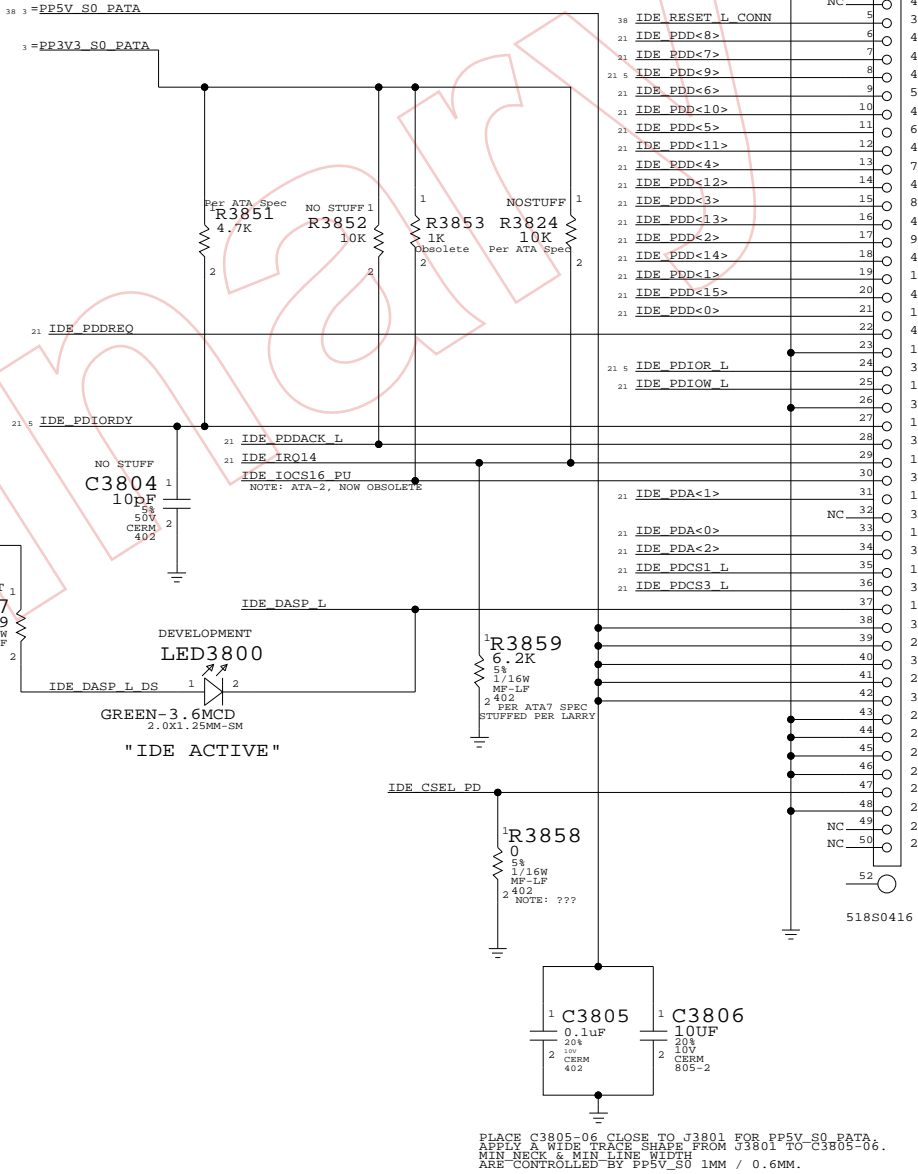
TP_SATA A R2D N

MAKE_BASE=TRUE

SATA A D2R P

MAKE_BASE=TRUE

SATA A D2R N

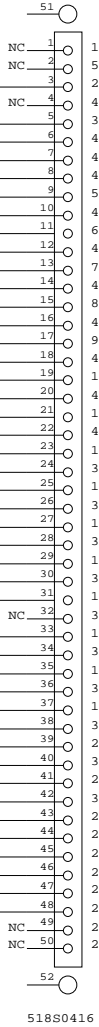


CRITICAL

J3801

87151-5005N

P-RT-SM



Disk Connectors

SYNC_MASTER=M51_D0UG

SYNC_DATE=08/04/2006

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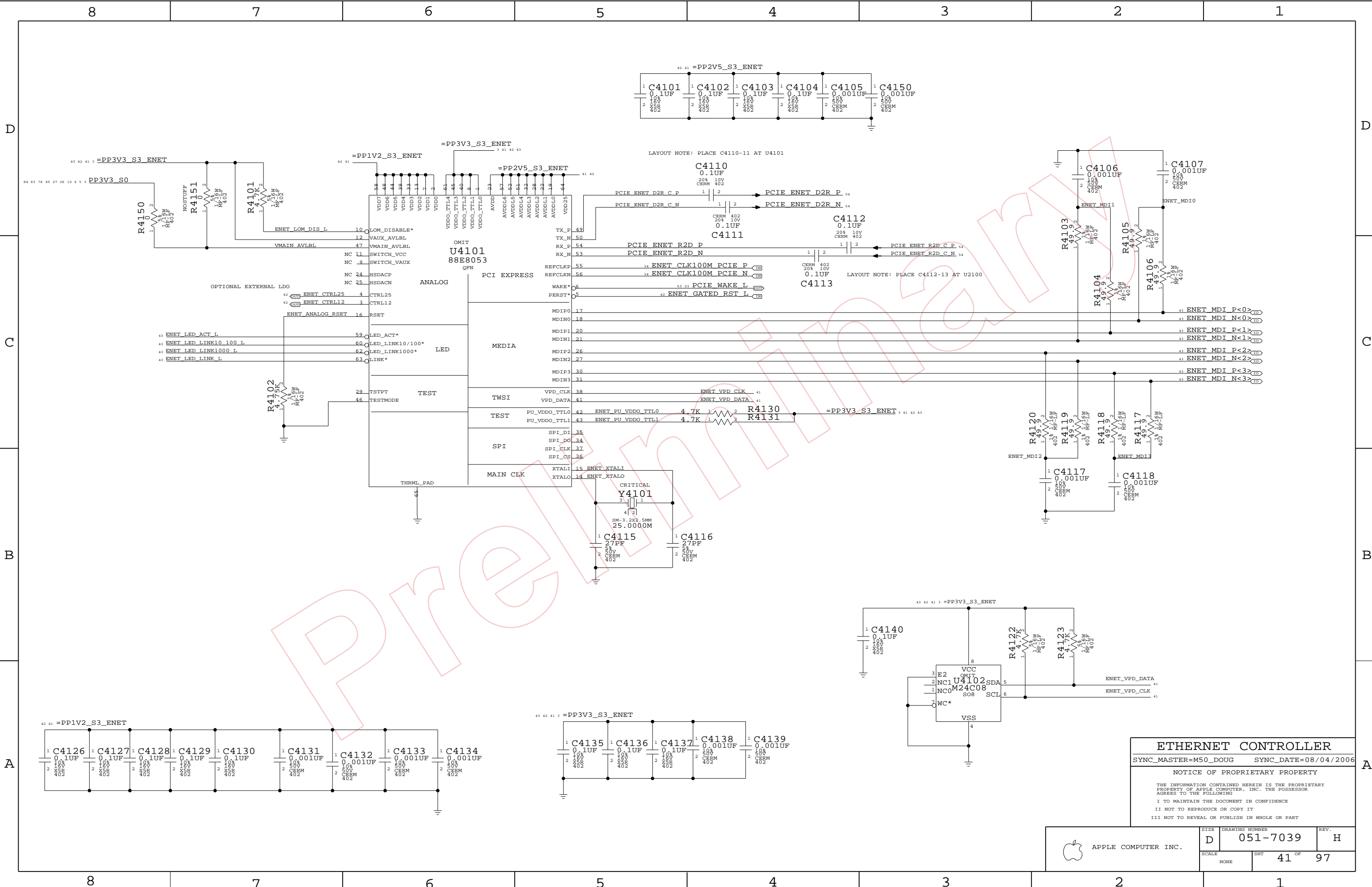
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SCALE

NONE

SHT

38 OF 97



ETHERNET CONTROLLER
SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

NOTICE OF PROPRIETARY PROPERTY

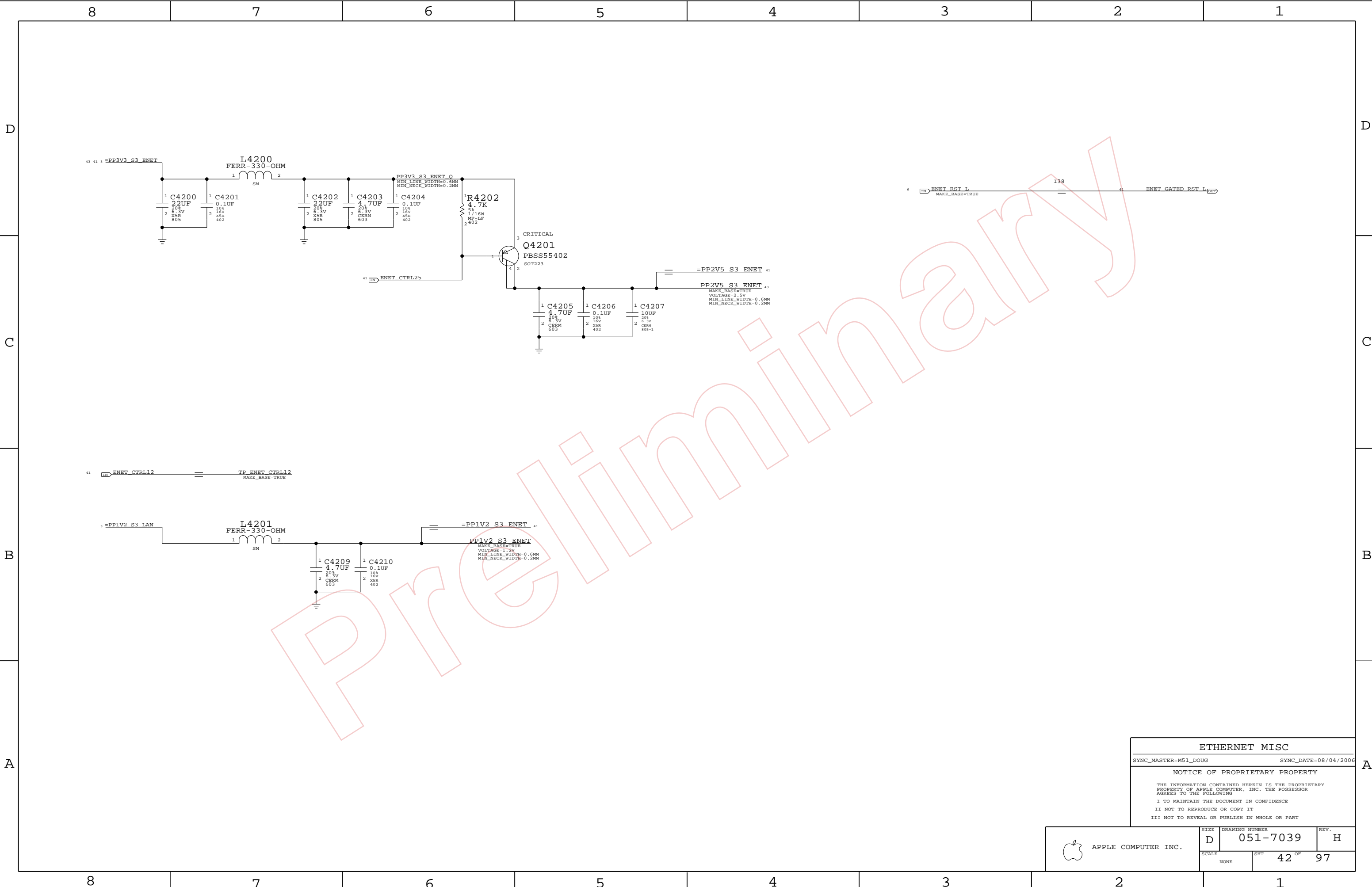
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ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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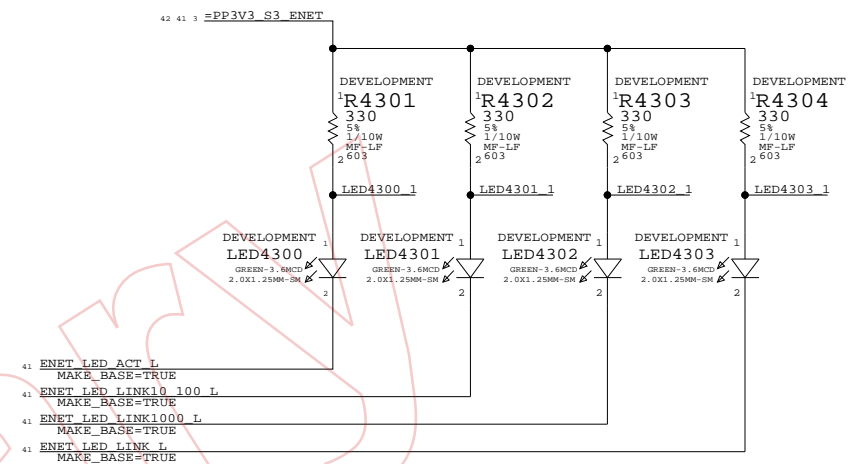
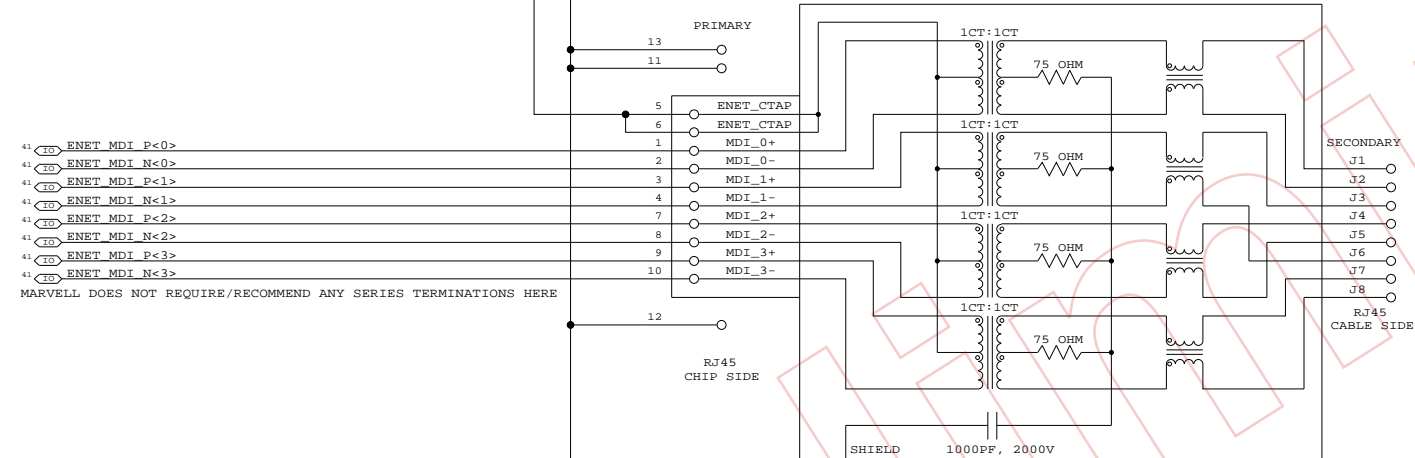
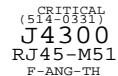
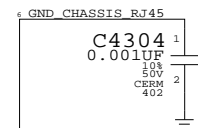
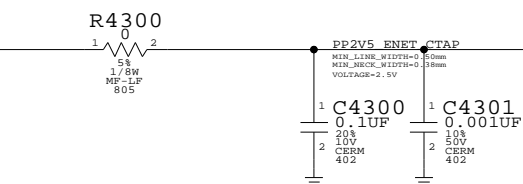
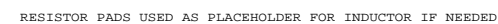
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NONE			



ETHERNET CONNECTOR

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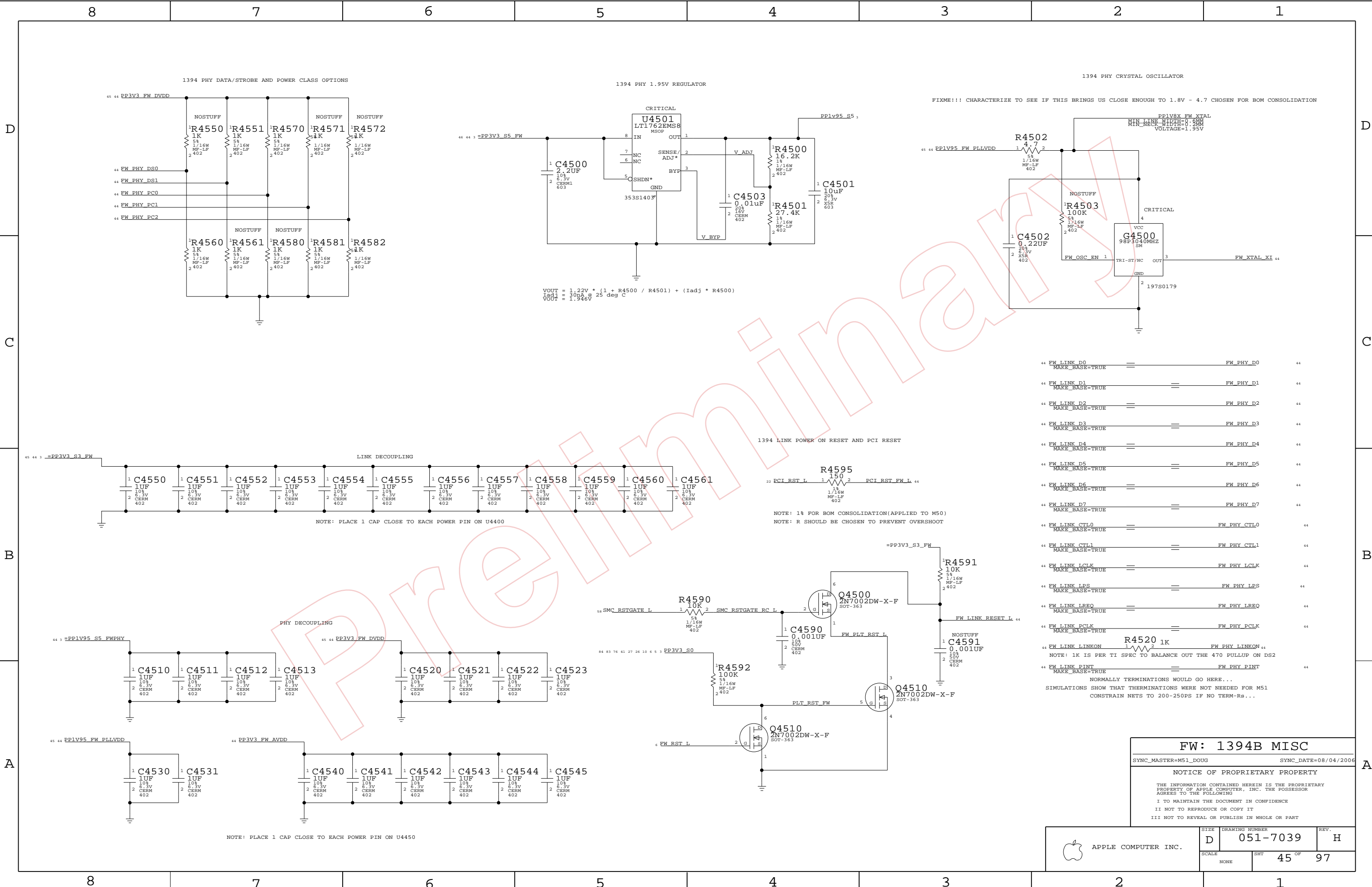
	SIZE
	D

SIZE	DRAWING NUMBER
D	051-

REV.

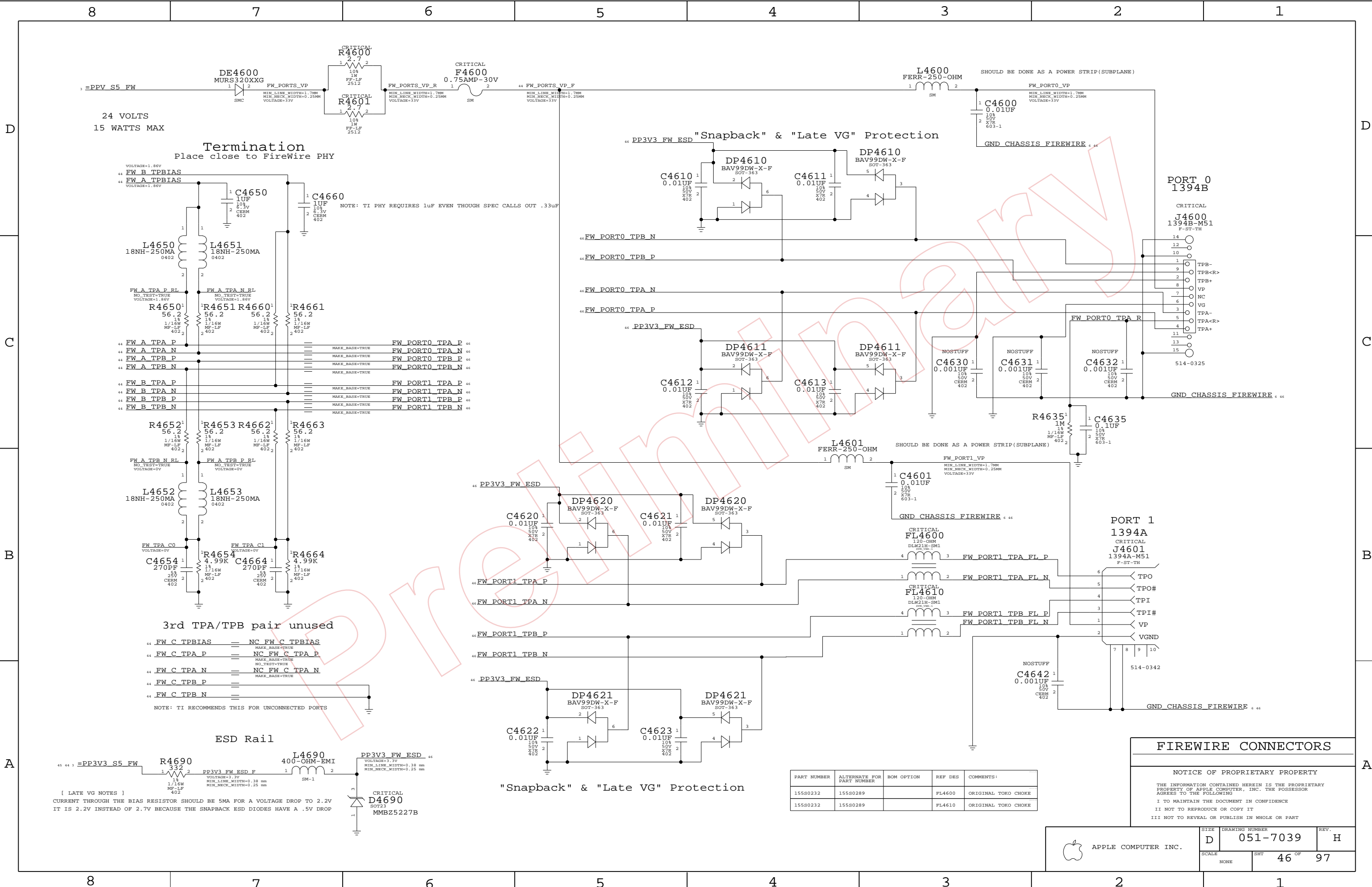
SCALE	NONE
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SHT 43 OF 97



FW: 1394B MISC		
SYNC_MASTER=M51_DOUG	SYNC_DATE=08/04/2006	
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FIREWIRE CONNECTORS

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

 APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7039	REV. H
SCALE NONE	SHT 46 OF 97	

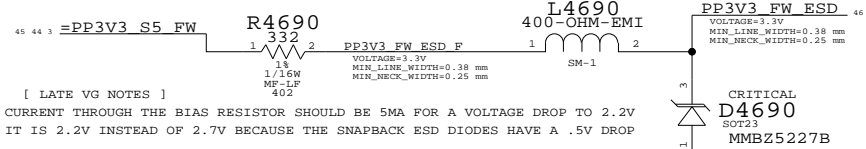
"Snapback" & "Late VG" Protection

ESD Rail

3rd TPA/TPB pair unused

- FW C TPBIAS = NC FW C TPBIAS
- FW C TPA P = NC FW C TPA P
- FW C TPA N = NC FW C TPA N
- FW C TPB P =
- FW C TPB N =

NOTE: TI RECOMMENDS THIS FOR UNCONNECTED PORTS

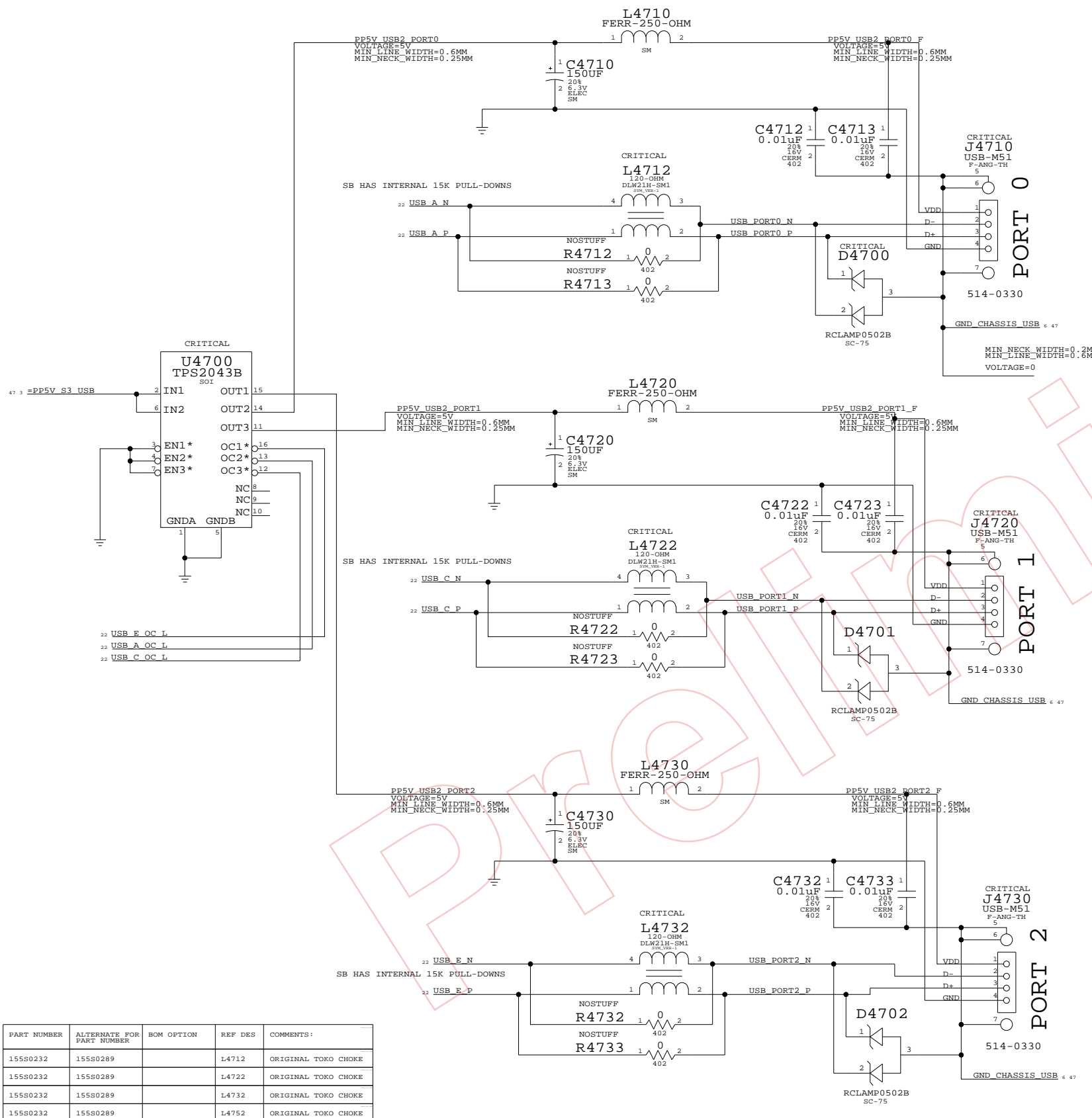


PORT 1
1394A
CRITICAL
J4601
1394A-M51
F-ST-TH

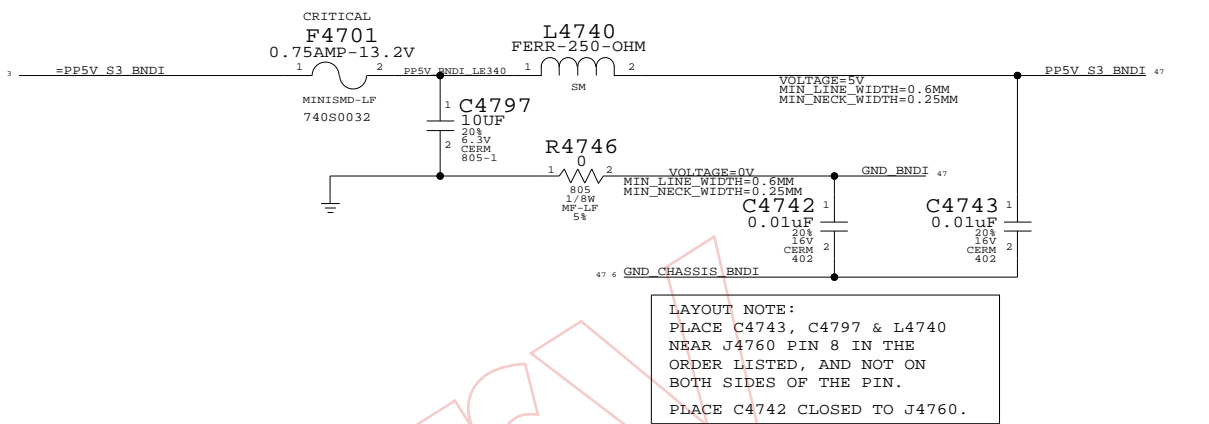
PORT 0
1394B

CRITICAL
J4600
1394B-M51
F-ST-TH

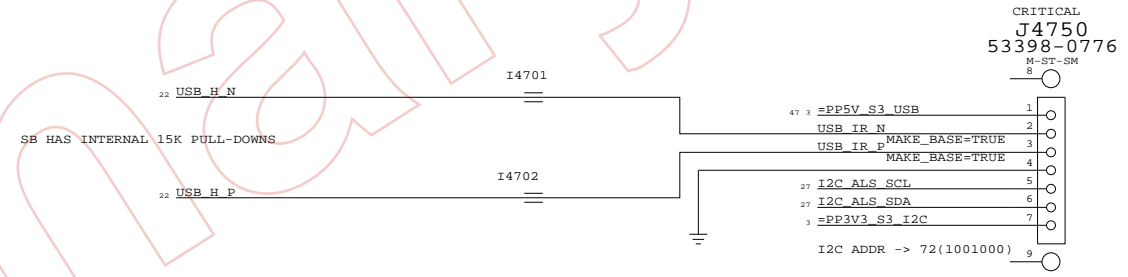
External USB Ports



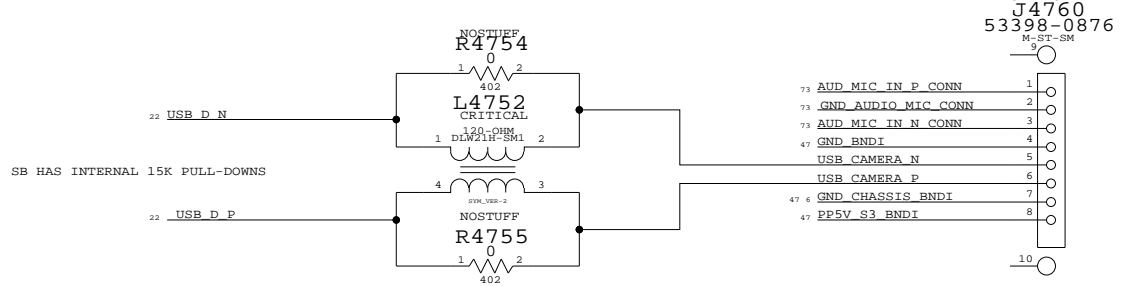
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155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



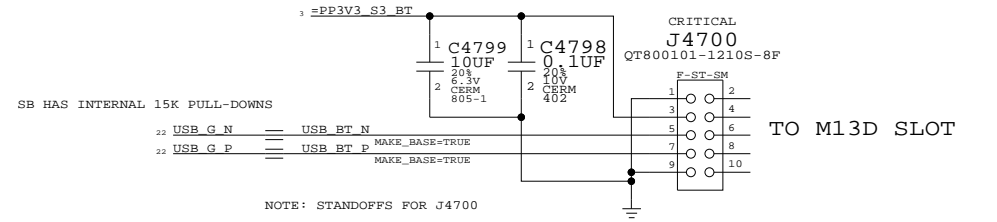
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



TO M13D SLOT

USB Device Interfaces

SYNC_MASTER=M51_D0UG SYNC_DATE=08/04/2006

NOTICE OF PROPRIETARY PROPERTY

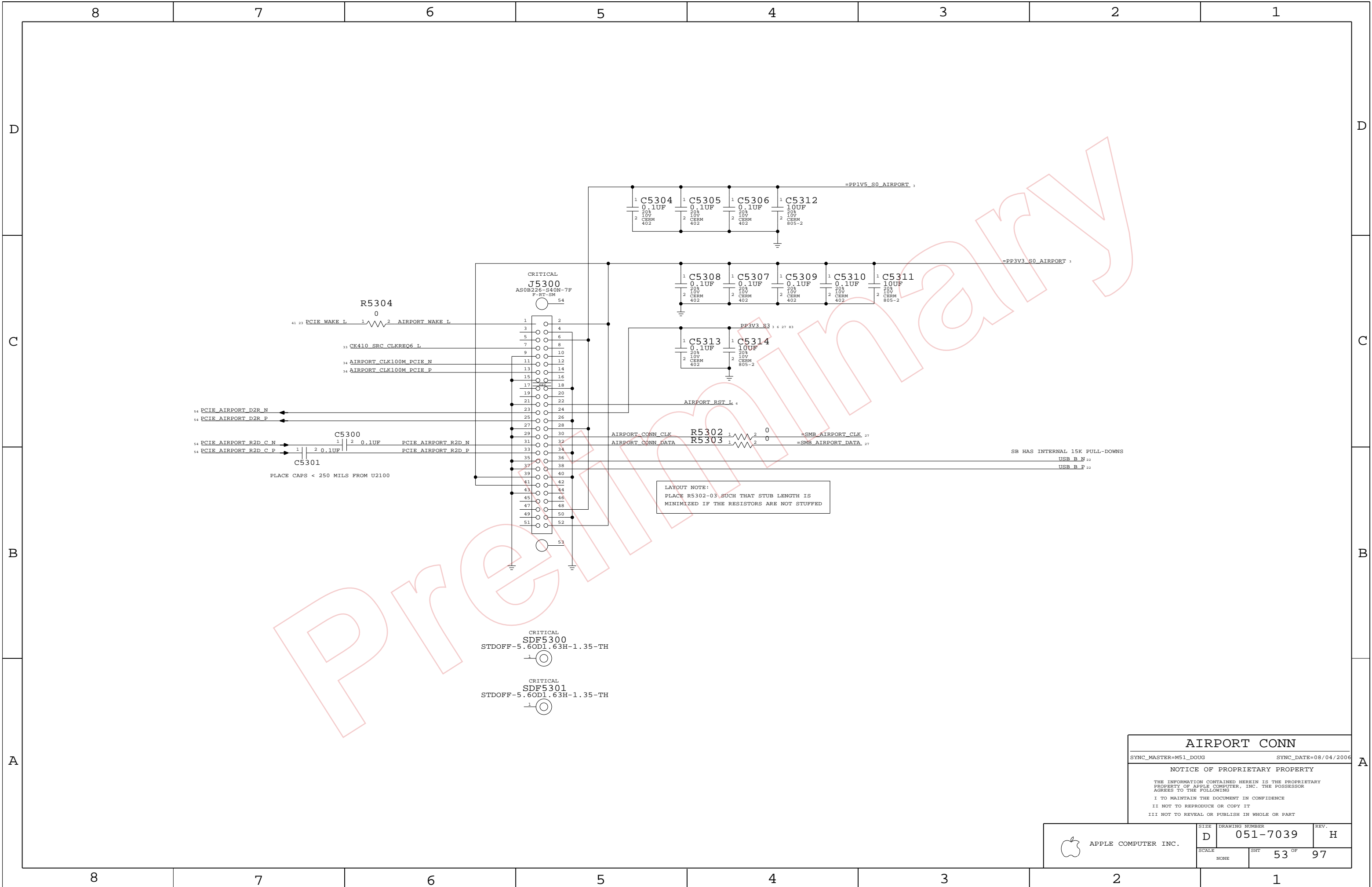
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AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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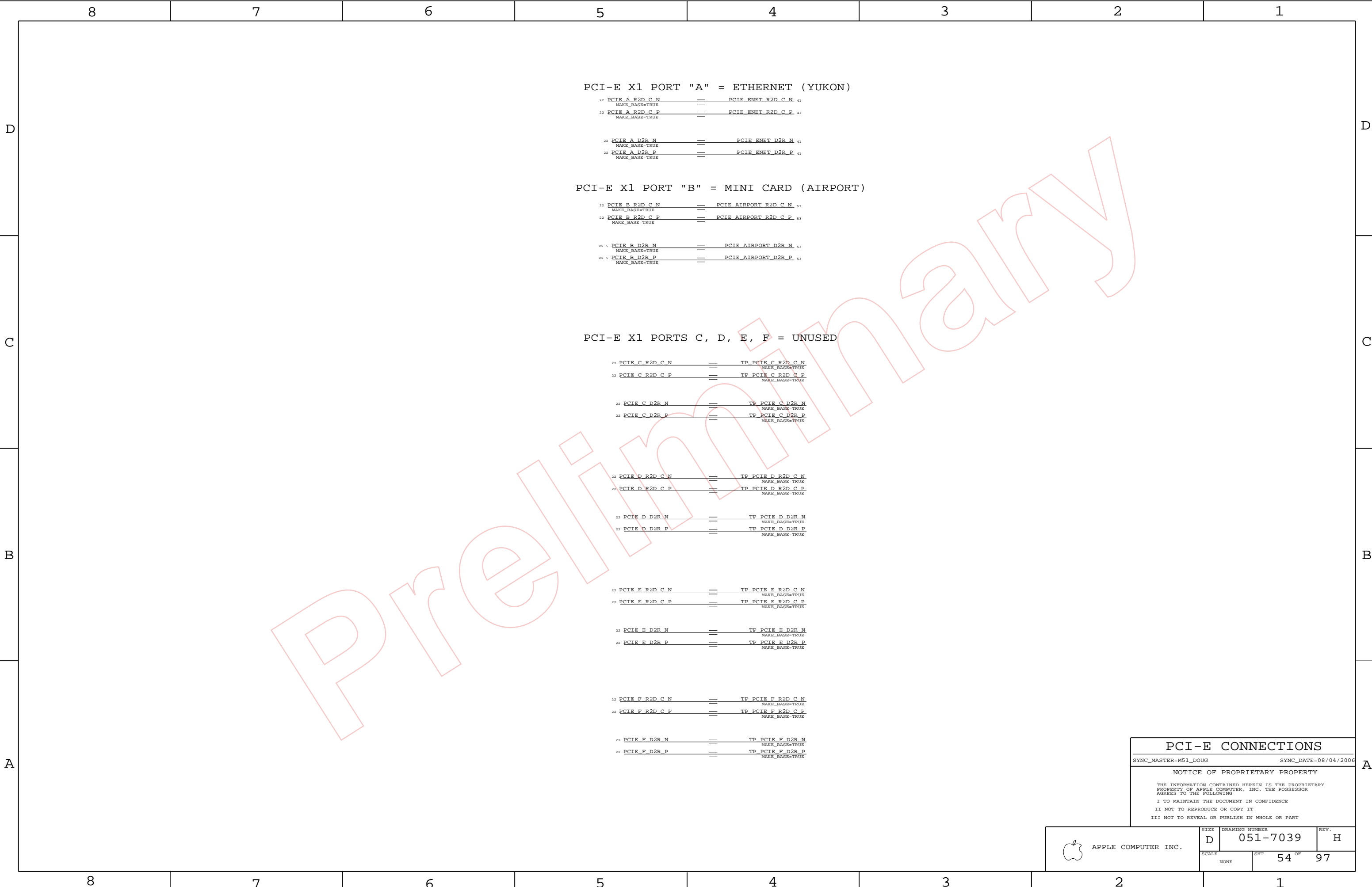
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7039 REV. H

SCALE NONE SHT 53 OF 97



22

PCIE A D2R P

MAKE_BASE=TRUE

PCIE ENET D2R P

41

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22

PCIE B R2D C N

MAKE_BASE=TRUE

PCIE AIRPORT R2D C N

53

22

PCIE B R2D C P

MAKE_BASE=TRUE

PCIE AIRPORT R2D C P

53

22

PCIE B D2R N

MAKE_BASE=TRUE

PCIE AIRPORT D2R N

53

22

PCIE B D2R P

MAKE_BASE=TRUE

PCIE AIRPORT D2R P

53

PCI-E X1 PORTS C, D, E, F = UNUSED

22

PCIE C R2D C N

MAKE_BASE=TRUE

TP PCIE C R2D C N

MAKE_BASE=TRUE

22

PCIE C R2D C P

MAKE_BASE=TRUE

TP PCIE C R2D C P

MAKE_BASE=TRUE

22

PCIE C D2R N

MAKE_BASE=TRUE

TP PCIE C D2R N

MAKE_BASE=TRUE

22

PCIE C D2R P

MAKE_BASE=TRUE

TP PCIE C D2R P

MAKE_BASE=TRUE

22

PCIE D R2D C N

MAKE_BASE=TRUE

TP PCIE D R2D C N

MAKE_BASE=TRUE

22

PCIE D R2D C P

MAKE_BASE=TRUE

TP PCIE D R2D C P

MAKE_BASE=TRUE

22

PCIE D D2R N

MAKE_BASE=TRUE

TP PCIE D D2R N

MAKE_BASE=TRUE

22

PCIE D D2R P

MAKE_BASE=TRUE

TP PCIE D D2R P

MAKE_BASE=TRUE

22

PCIE E R2D C N

MAKE_BASE=TRUE

TP PCIE E R2D C N

MAKE_BASE=TRUE

22

PCIE E R2D C P

MAKE_BASE=TRUE

TP PCIE E R2D C P

MAKE_BASE=TRUE

22

PCIE E D2R N

MAKE_BASE=TRUE

TP PCIE E D2R N

MAKE_BASE=TRUE

22

PCIE E D2R P

MAKE_BASE=TRUE

TP PCIE E D2R P

MAKE_BASE=TRUE

22

PCIE F R2D C N

MAKE_BASE=TRUE

TP PCIE F R2D C N

MAKE_BASE=TRUE

22

PCIE F R2D C P

MAKE_BASE=TRUE

TP PCIE F R2D C P

MAKE_BASE=TRUE

22

PCIE F D2R N

MAKE_BASE=TRUE

TP PCIE F D2R N

MAKE_BASE=TRUE

22

PCIE F D2R P

MAKE_BASE=TRUE

TP PCIE F D2R P

MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG

SYNC_DATE=08/04/2006


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APPLE COMPUTER INC.

SIZE

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DRAWING NUMBER

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H

SCALE

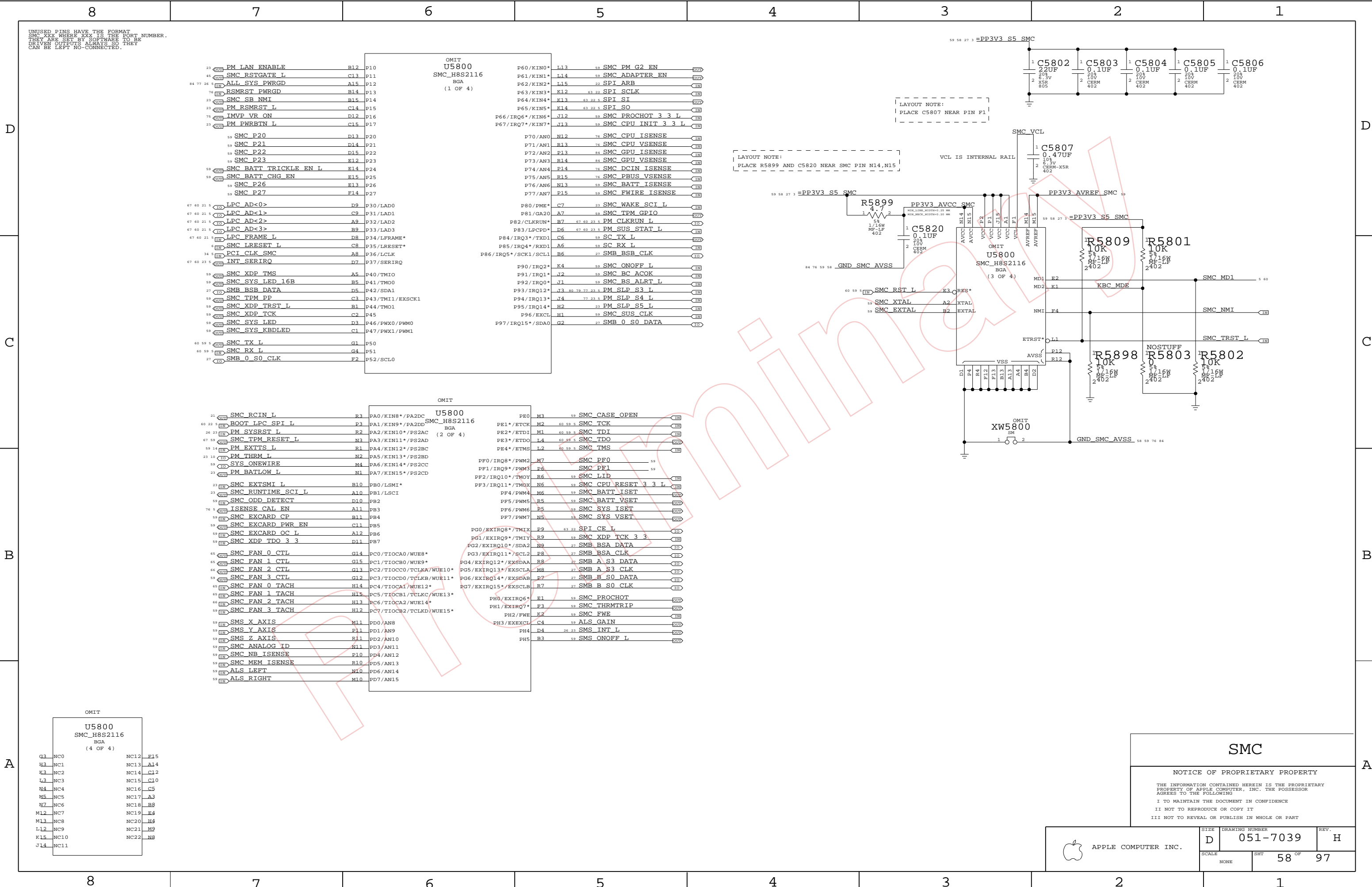
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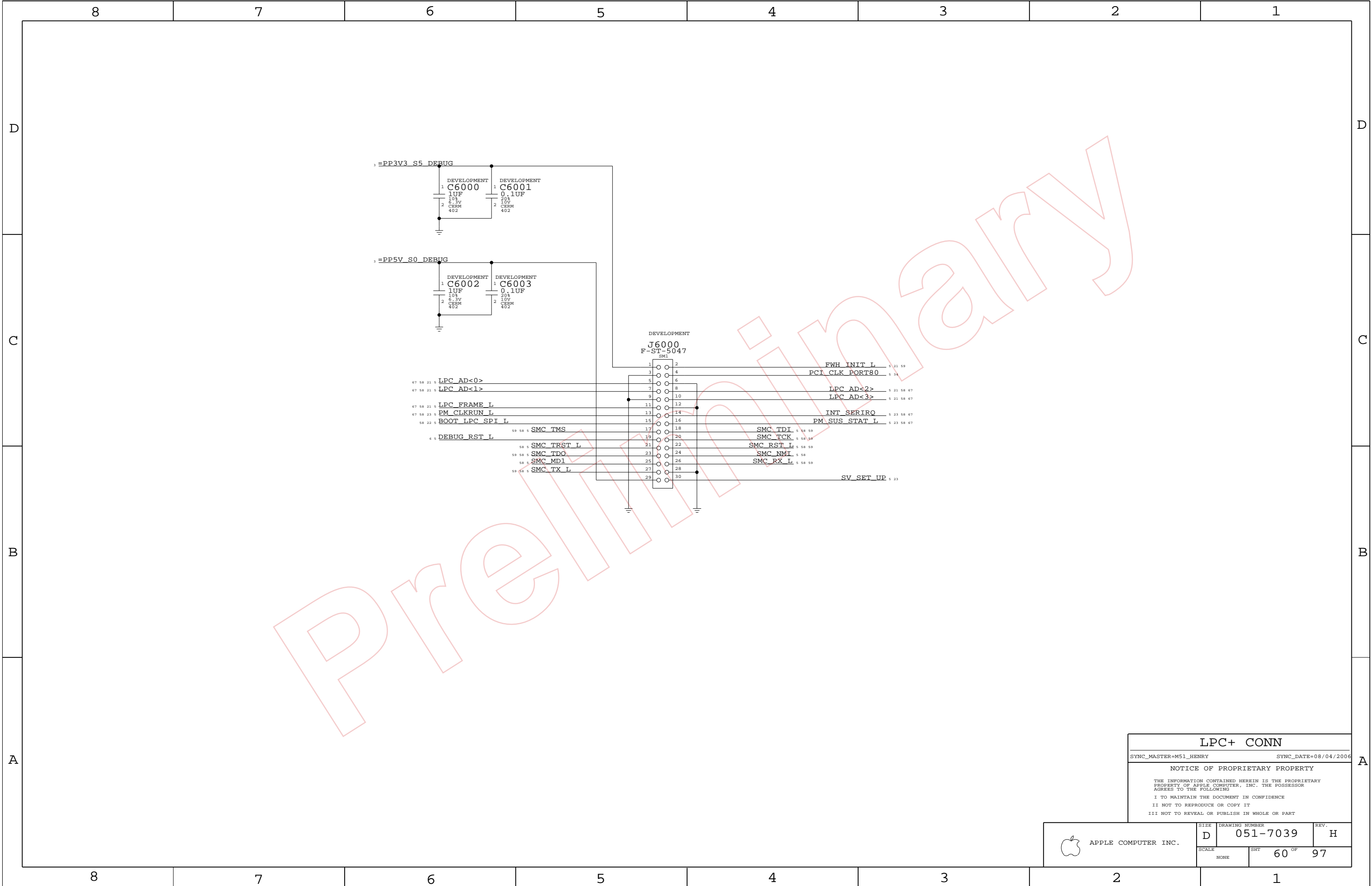
SHT

54

OF

97





LPC+ CONN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

NOTICE OF PROPRIETARY PROPERTY

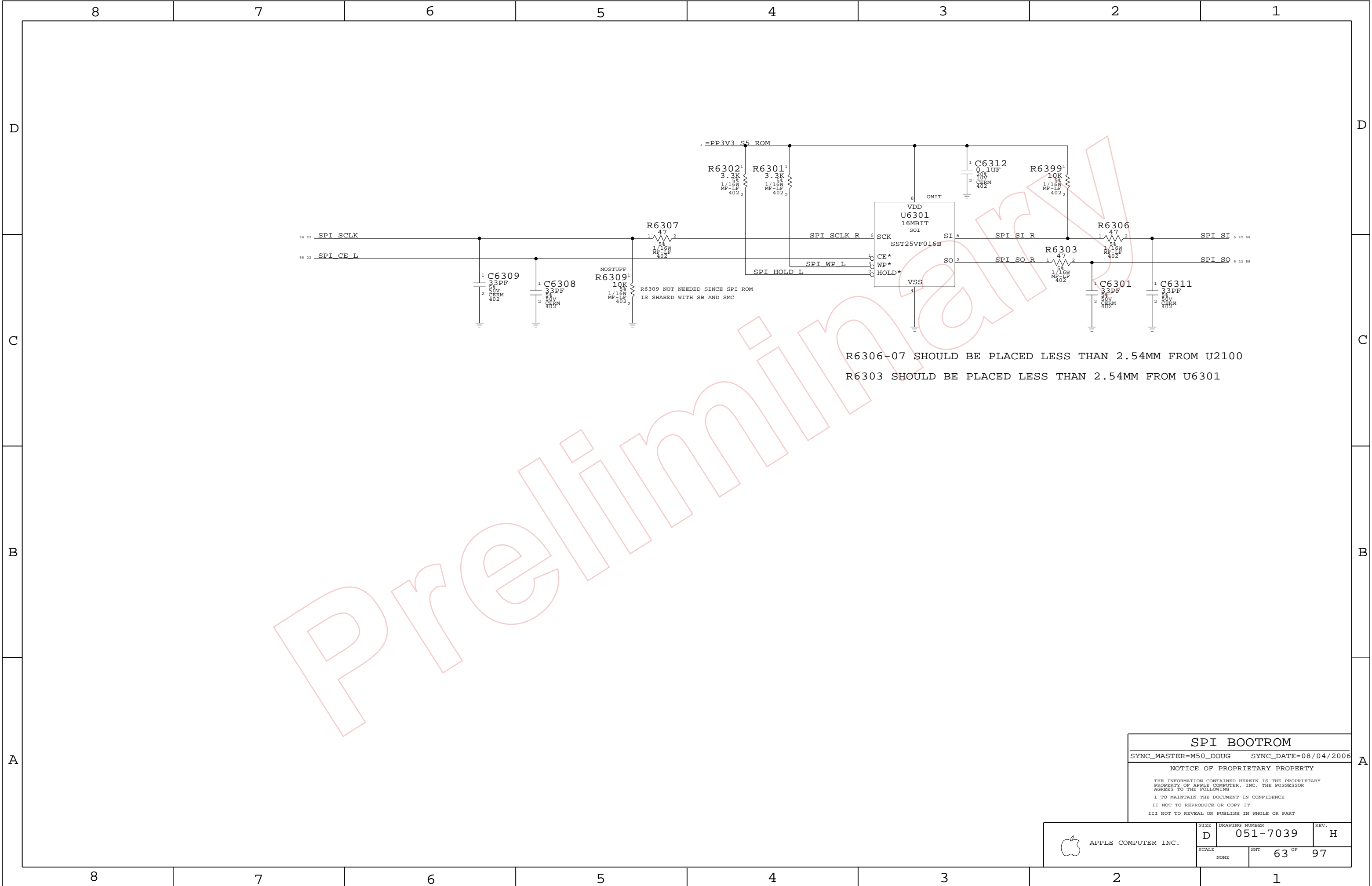
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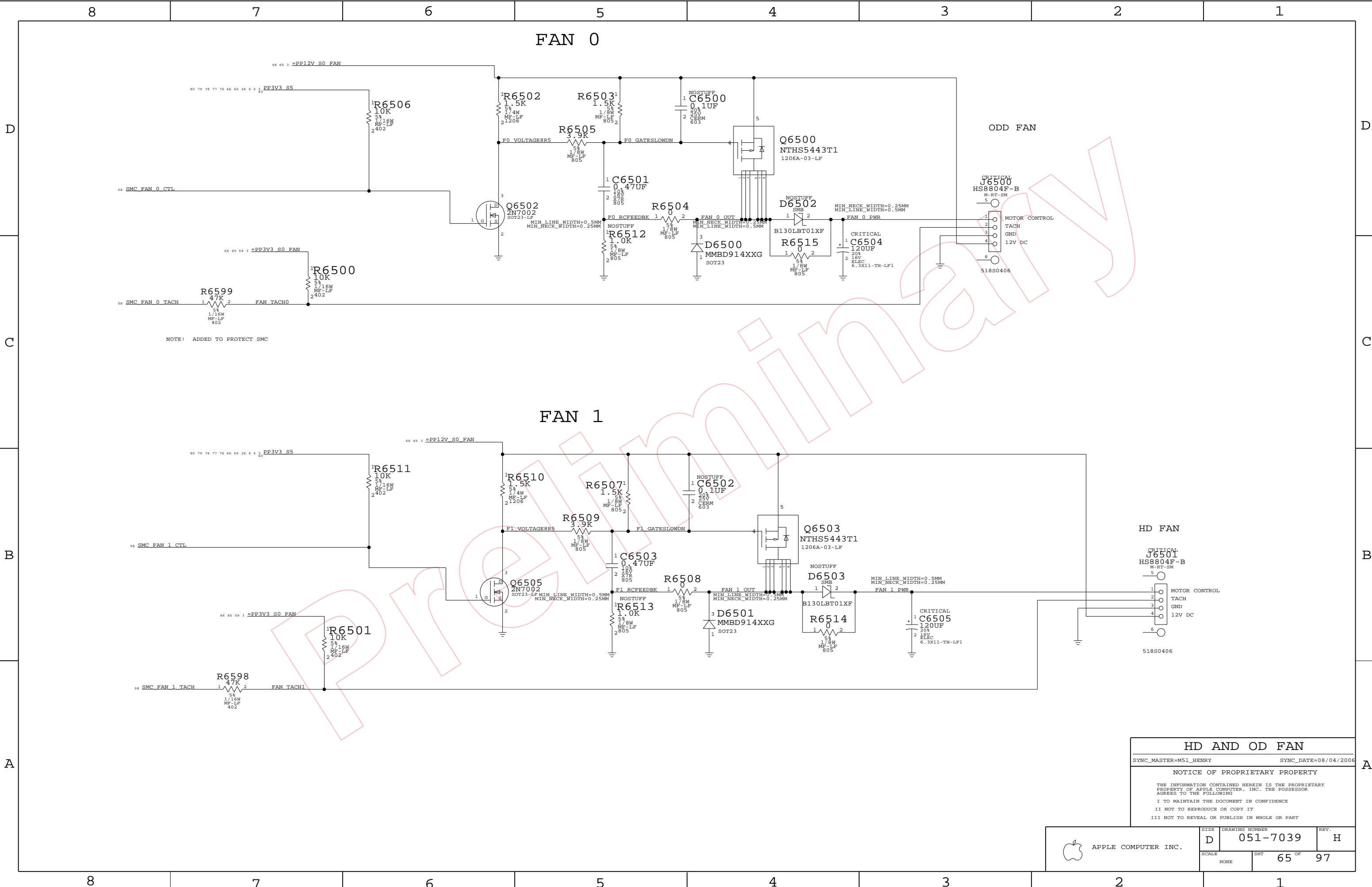
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HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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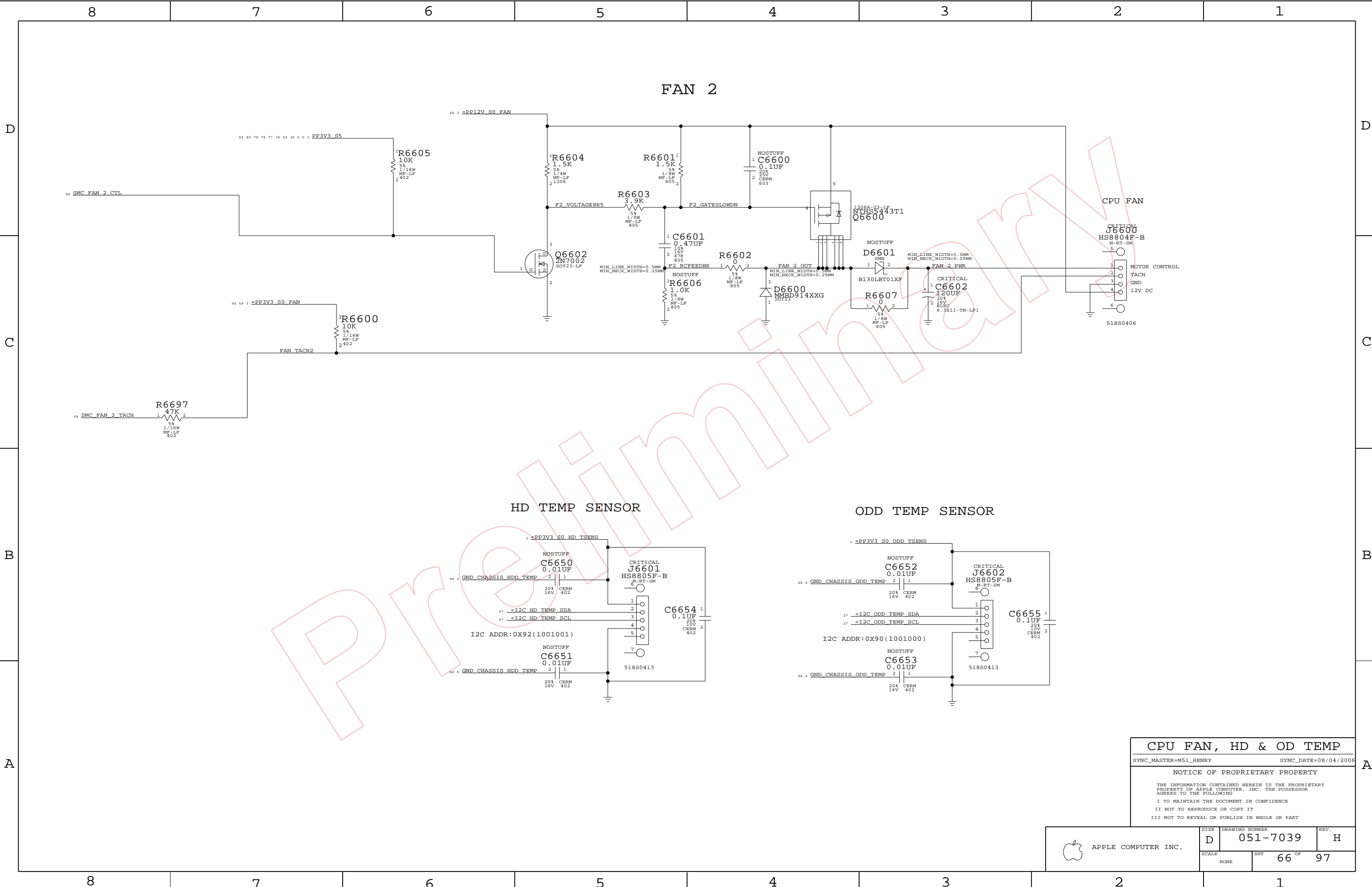
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NONE			



CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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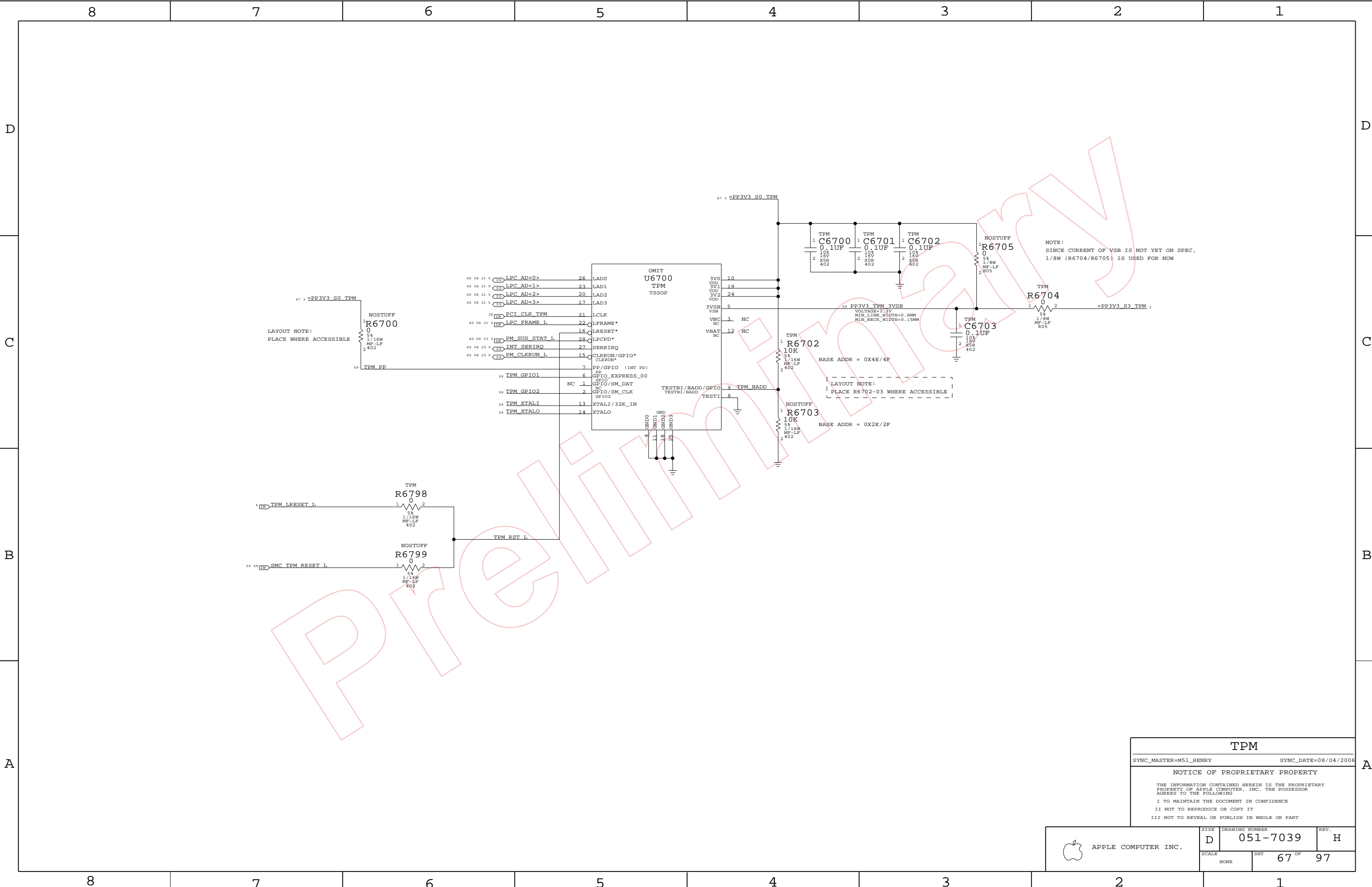
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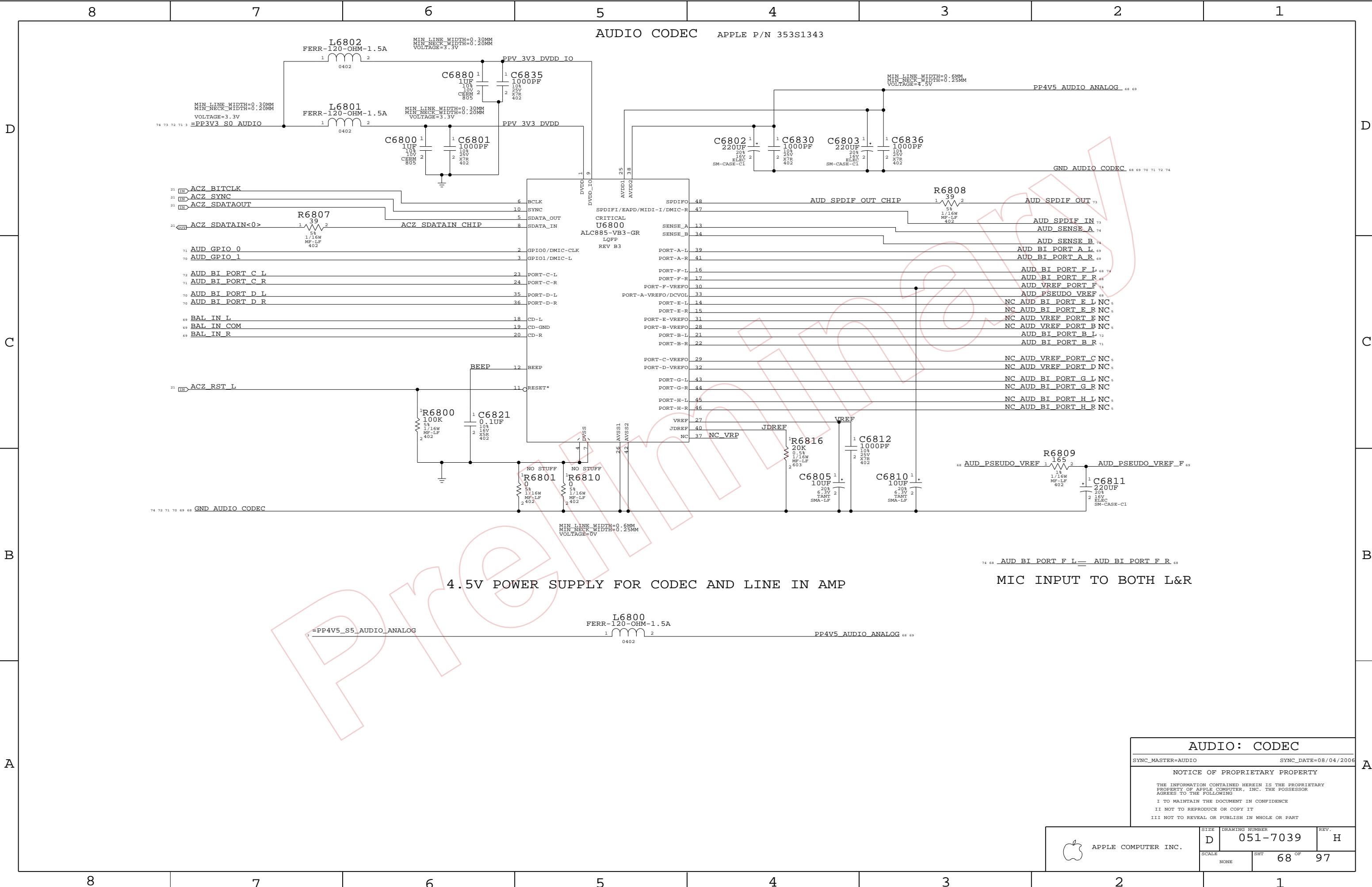
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SCALE		SHT	66 OF 97
NONE			



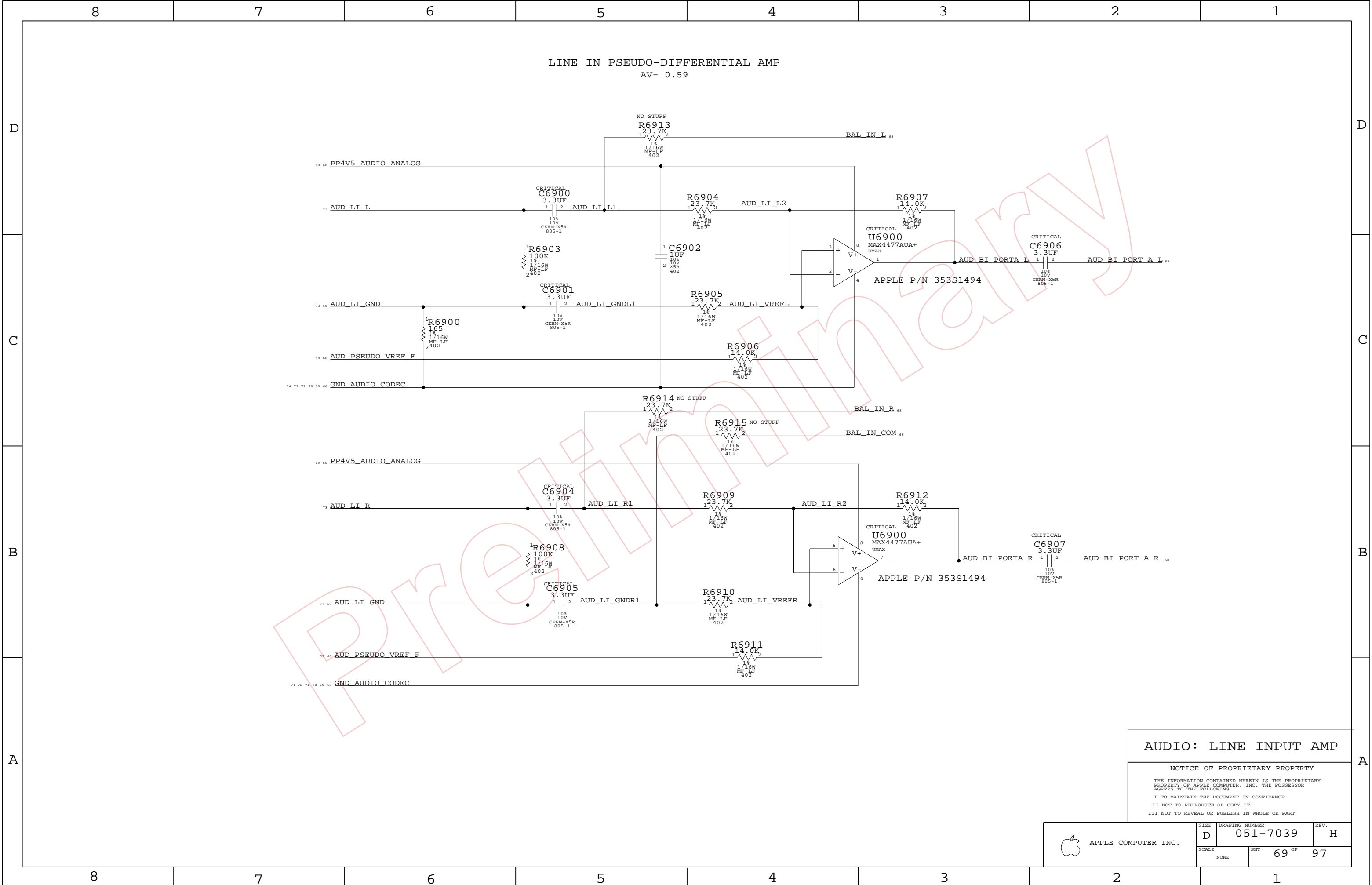
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SYNC_MASTER=M51_HENRY		SYNC_DATE=08/04/2006
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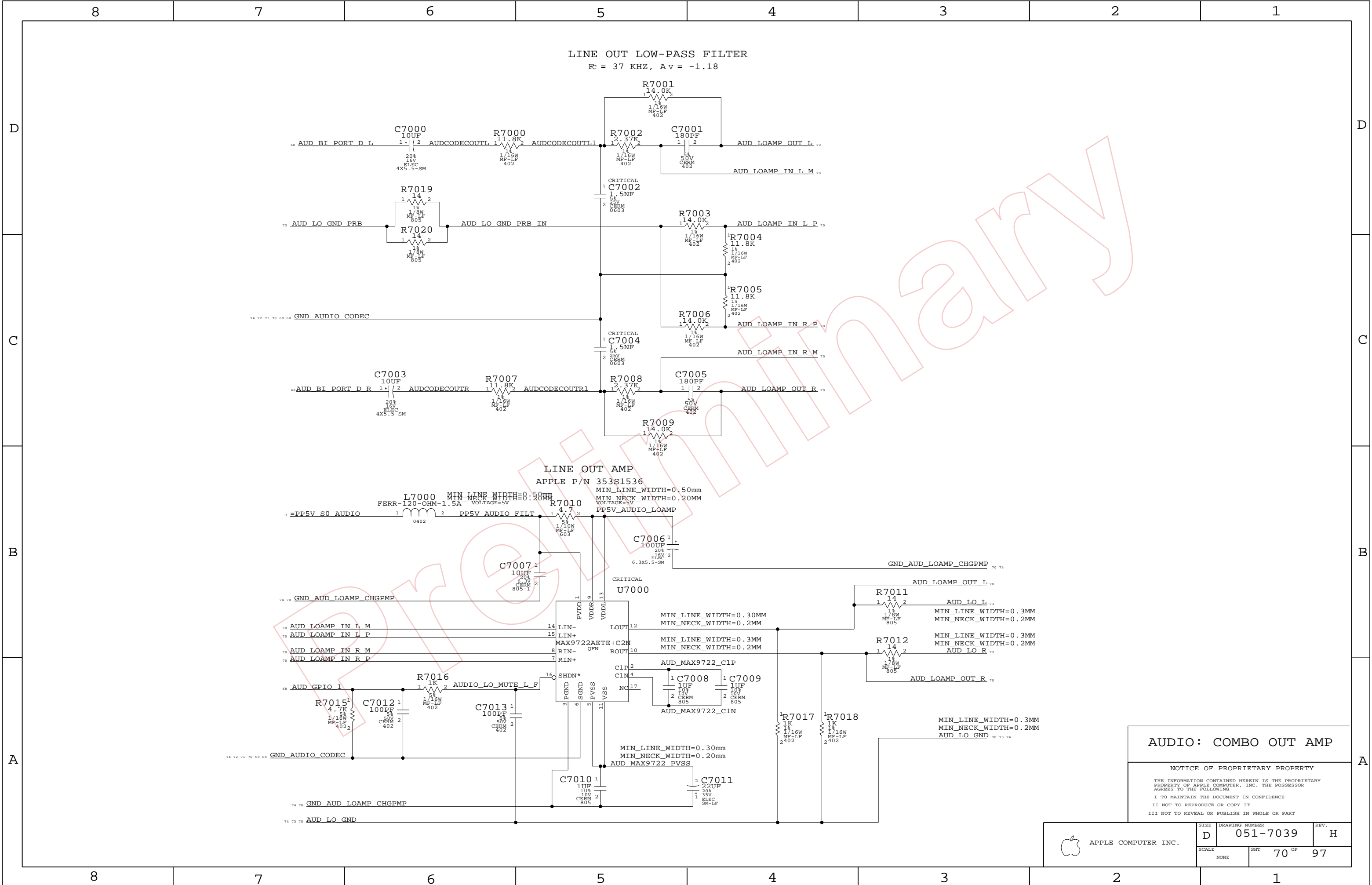
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NONE			

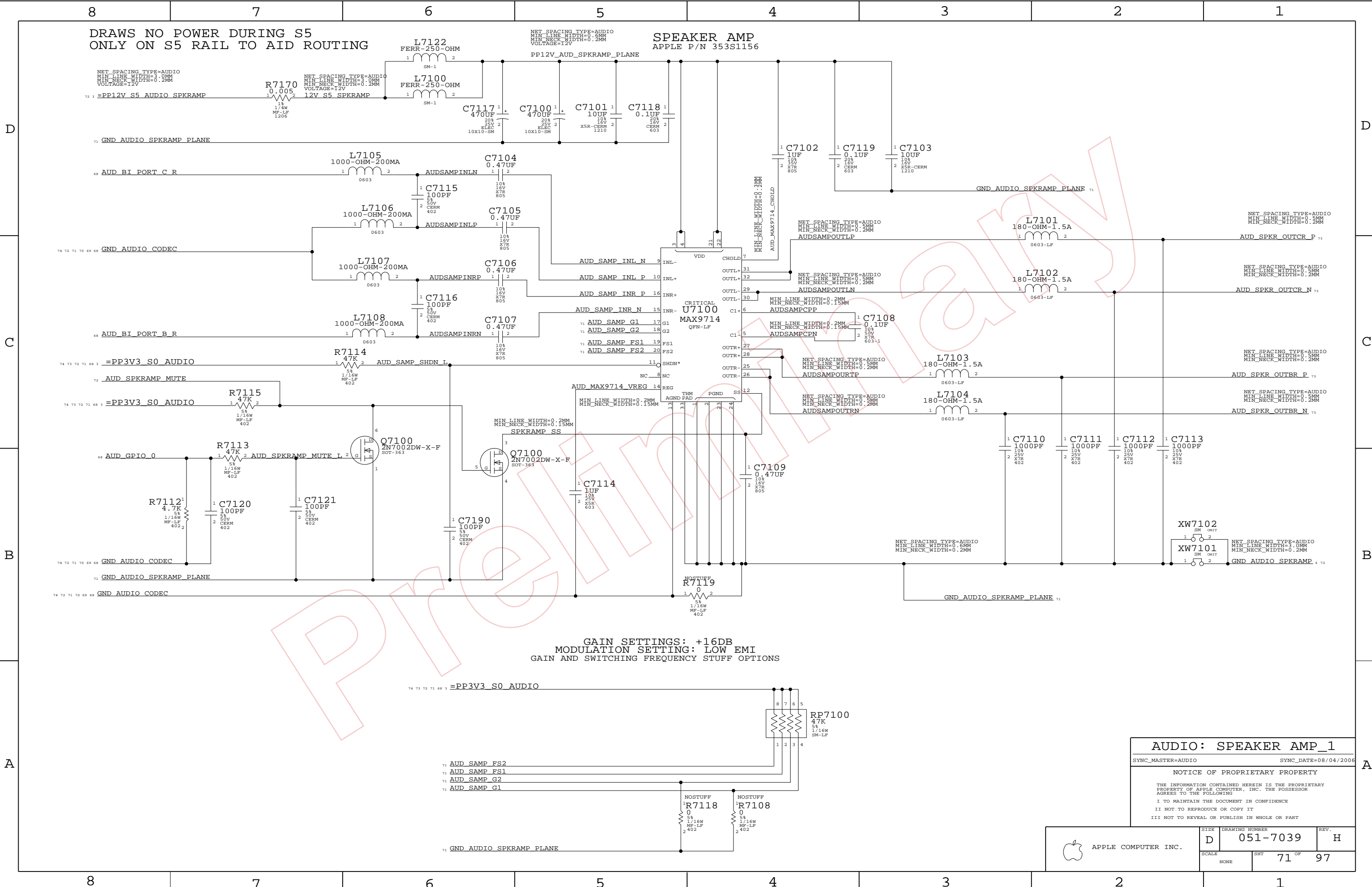


AUDIO: CODEC		
SYNC_MASTER=AUDIO		SYNC_DATE=08/04/2006
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SCALE	NONE	SHT	68 OF 97







AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO

SYNC_DATE=08/04/2006

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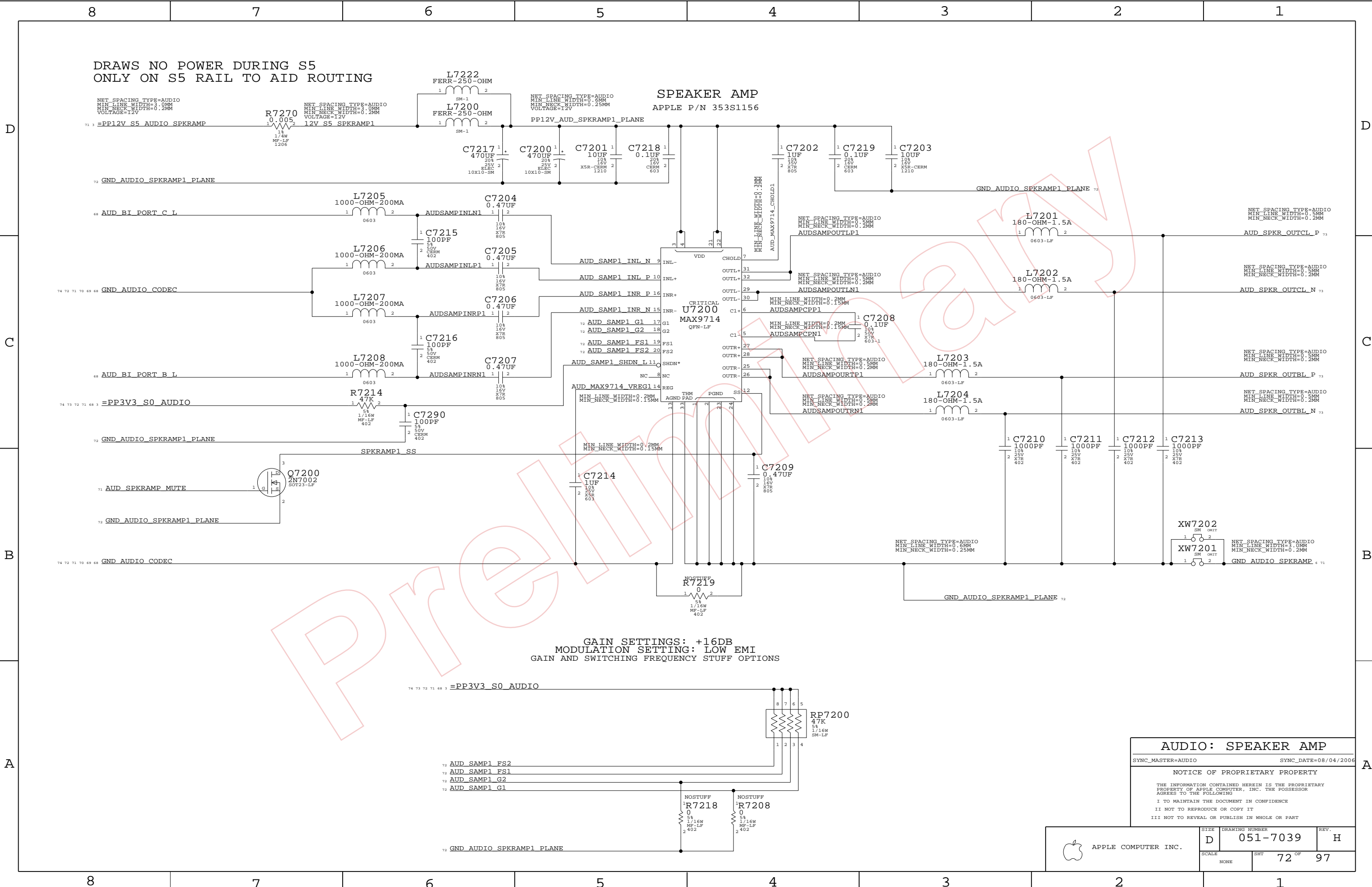
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SCALE	SHT		
	71 OF 97		



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO

SYNC_DATE=08/04/2006

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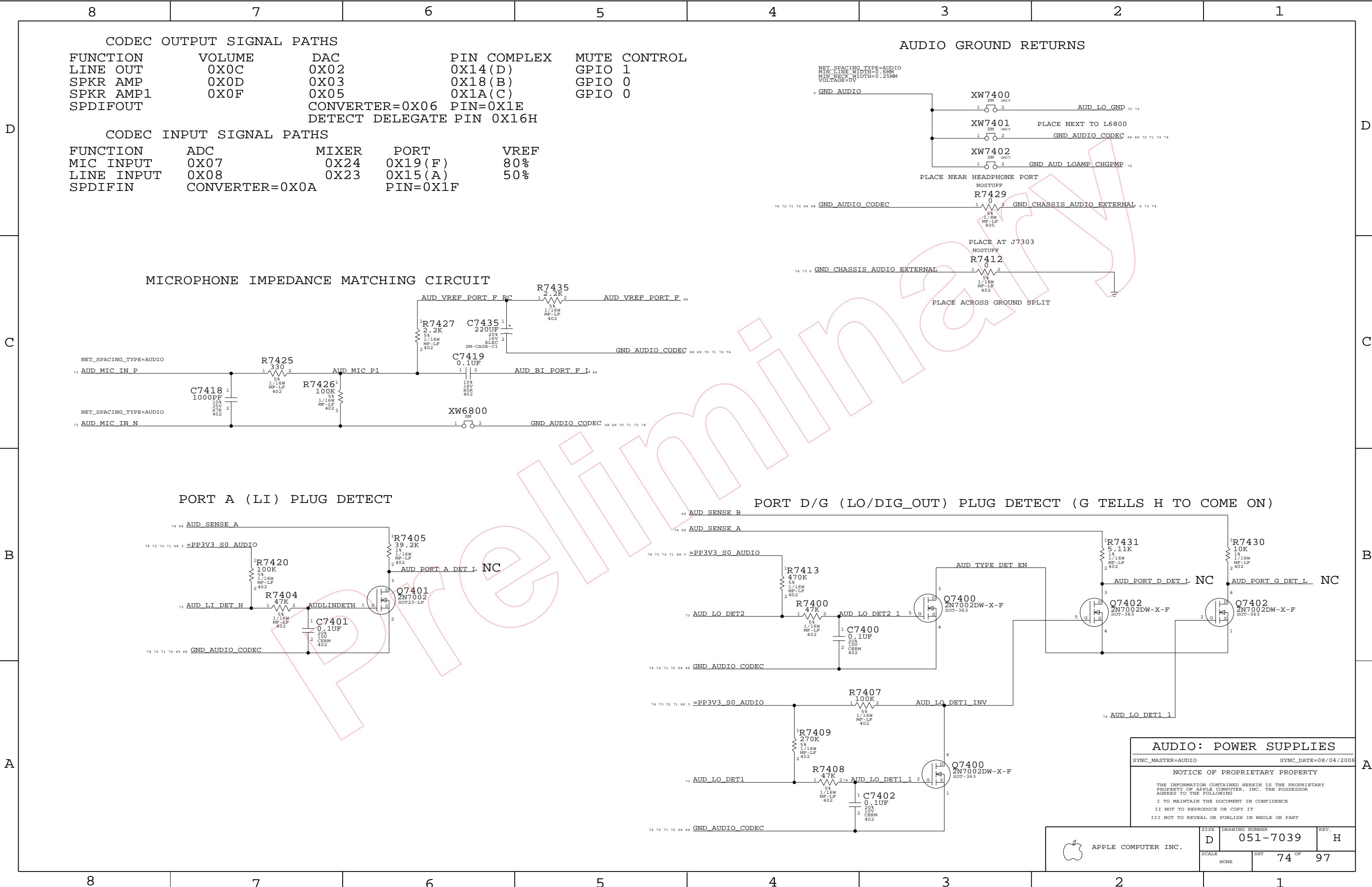
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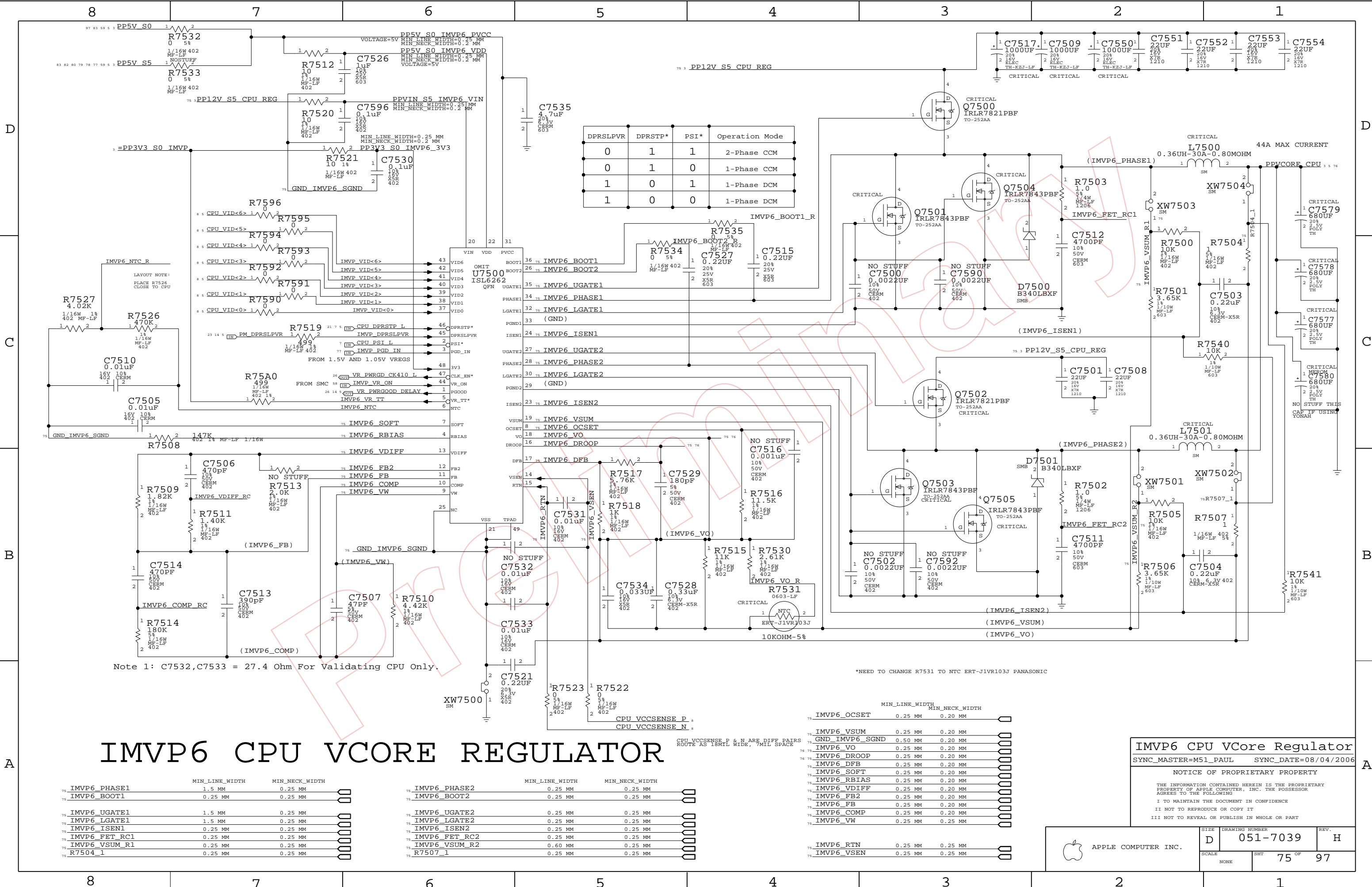
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	NONE		





IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

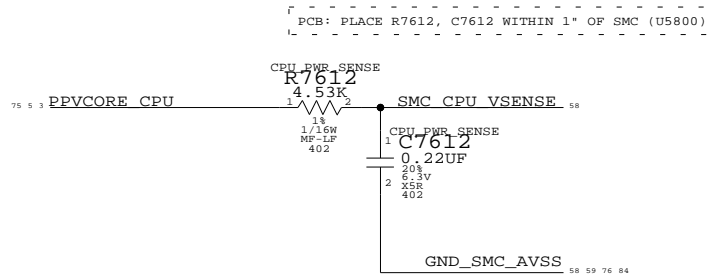
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
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IMVP6_RTIN	0.25 MM	0.25 MM
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IMVP6 CPU VCore Regulator
SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

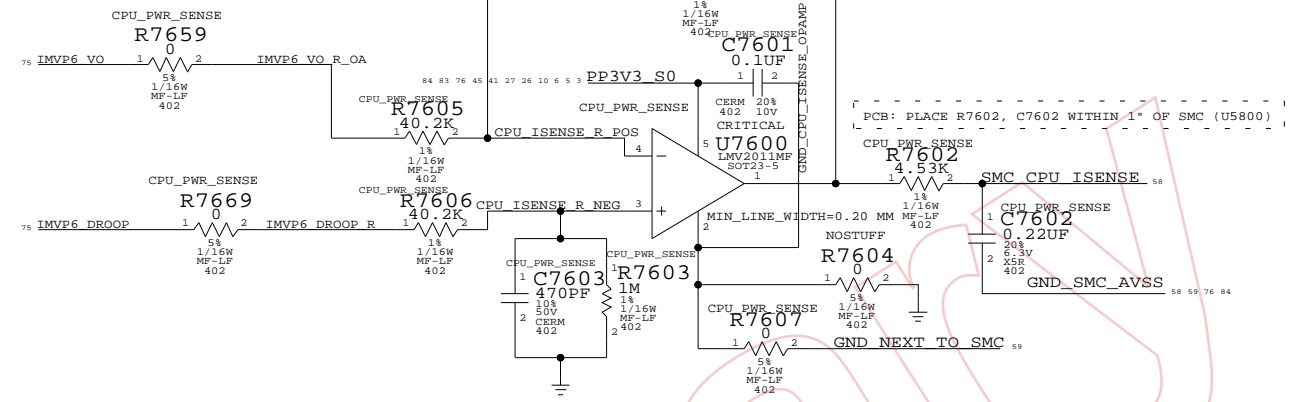
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SIZE	D	DRAWING NUMBER	051-7039	REV.	H
SCALE	NONE	SHT	75 OF 97		

PROCESSOR VCORE SENSE

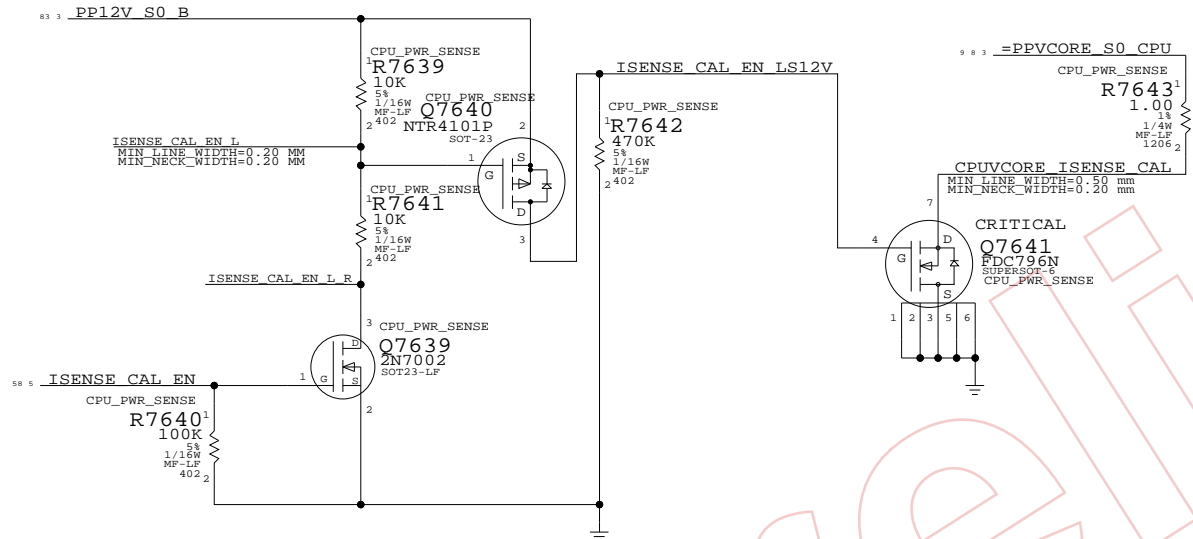


PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

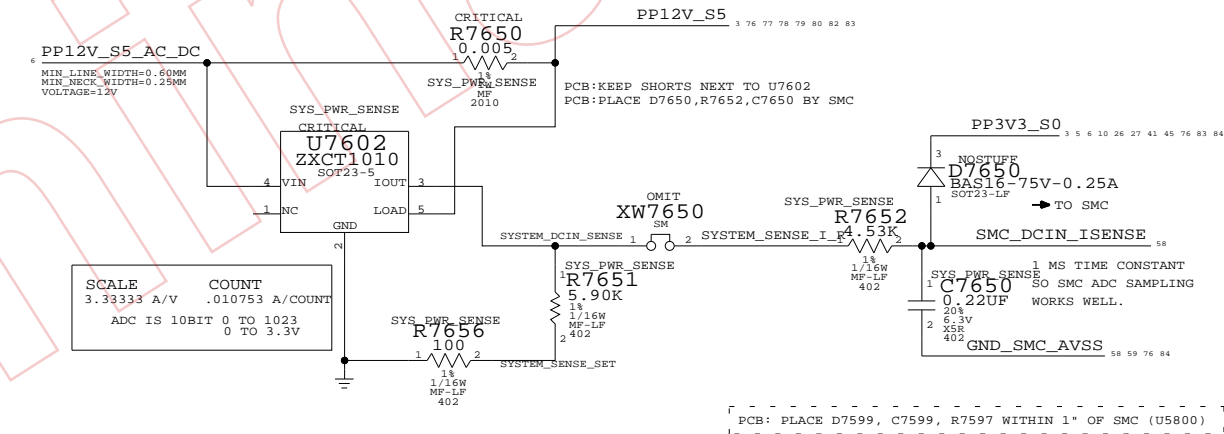


CPU CURRENT SENSE CALIBRATION CIRCUIT

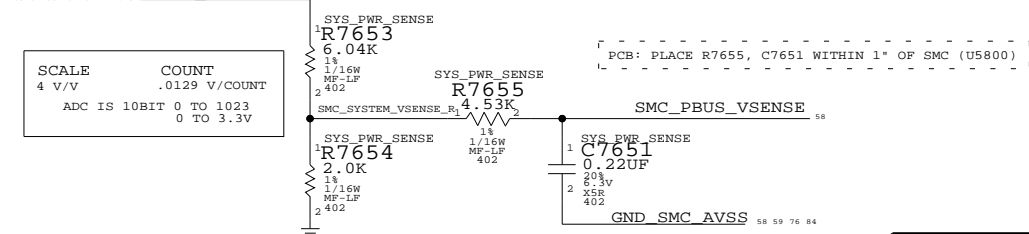
Switches in fixed load on power supplies to calibrate current sense circuits



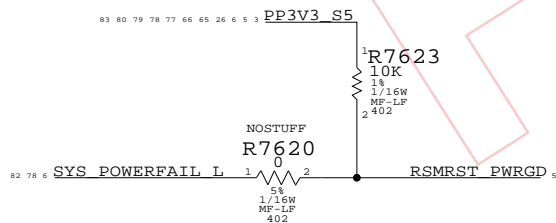
SYSTEM CURRENT SENSE



SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



SMC PWRGD PULLUP



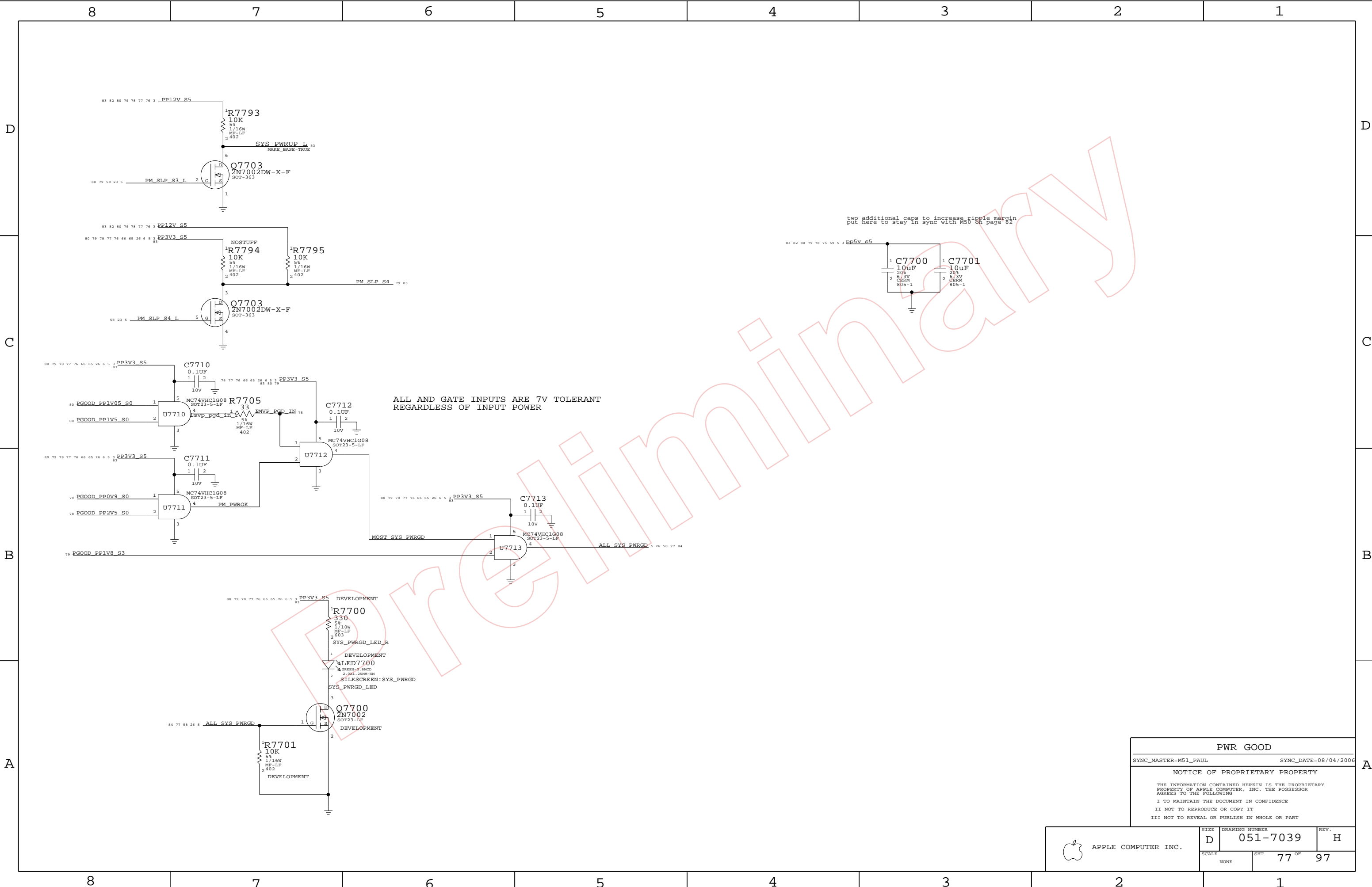
CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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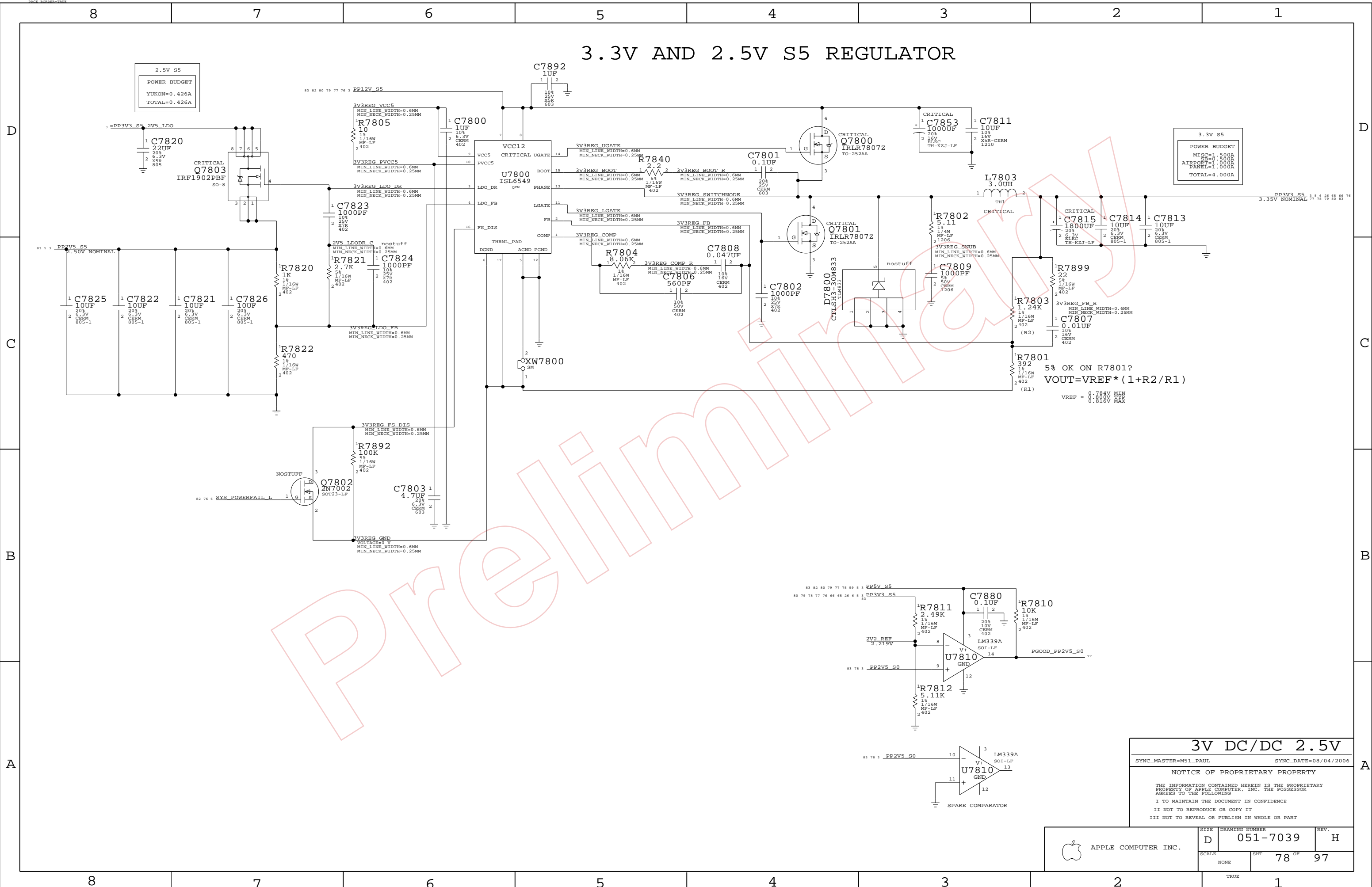
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	D	051-7039	H
SCALE		SHT	76 OF 97
NONE			



PWR_GOOD		
SYNC_MASTER=M51_PAUL		SYNC_DATE=08/04/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. H
	SCALE NONE	SHT 77 OF 97	



1.5V S0 AND 1.05V S0 RAILS

D

D

C

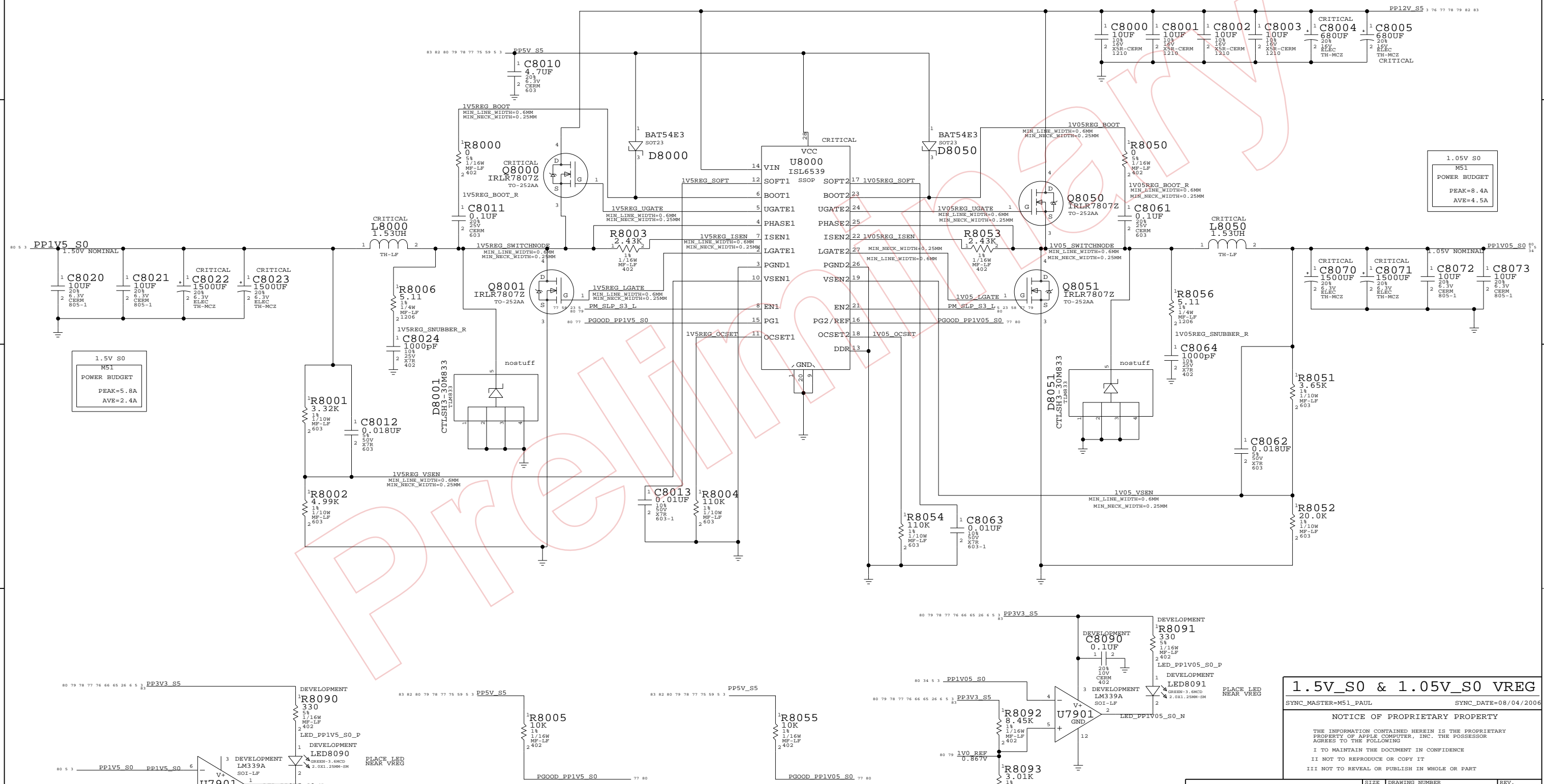
C

B

B

A

A



8

7

6

5

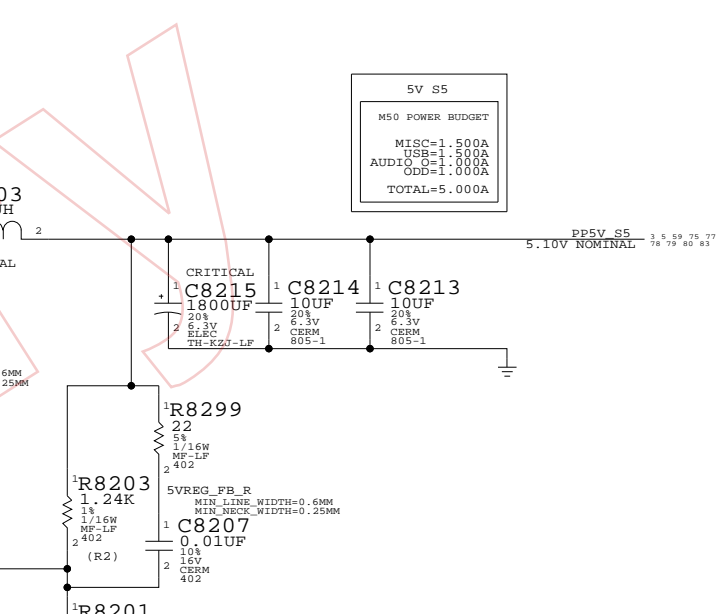
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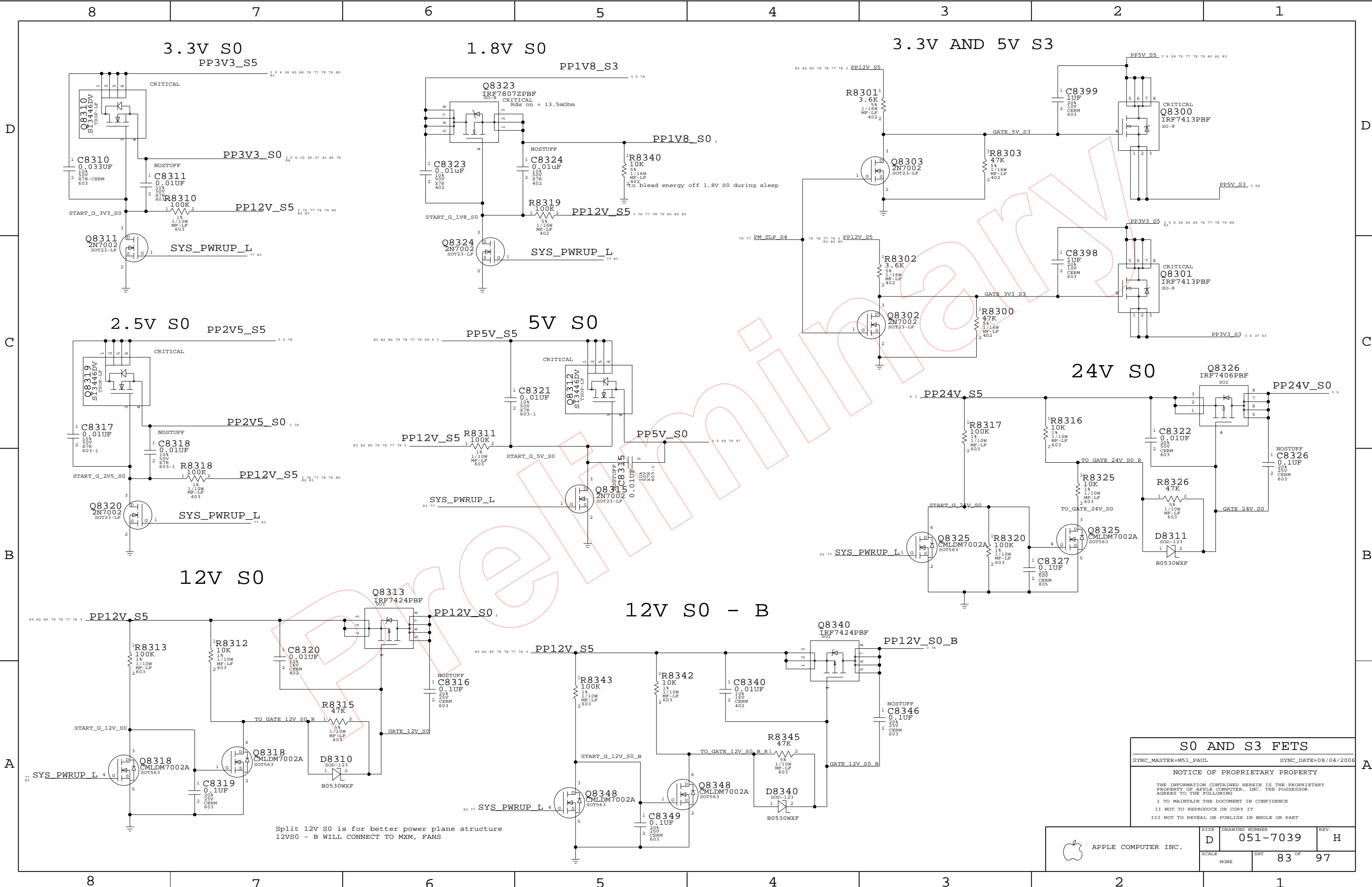
2

1

PCB layout for a 5V regulator circuit. The circuit includes a 5VREG FS DIS input, a 100K resistor (R8292), a 2N7002 MOSFET (Q8202), a 4.7uF capacitor (C8203), and a 5VREG GND output. The layout shows the placement of these components on a PCB with various pads and traces. A large red watermark 'P' is visible across the image.



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	H
	SCALE	SHT	OF
	NONE	82	97



S0 AND S3 FETS

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Split 12V S0 is for better power plane structure
12VS0 - B WILL CONNECT TO MXM, FANS

Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

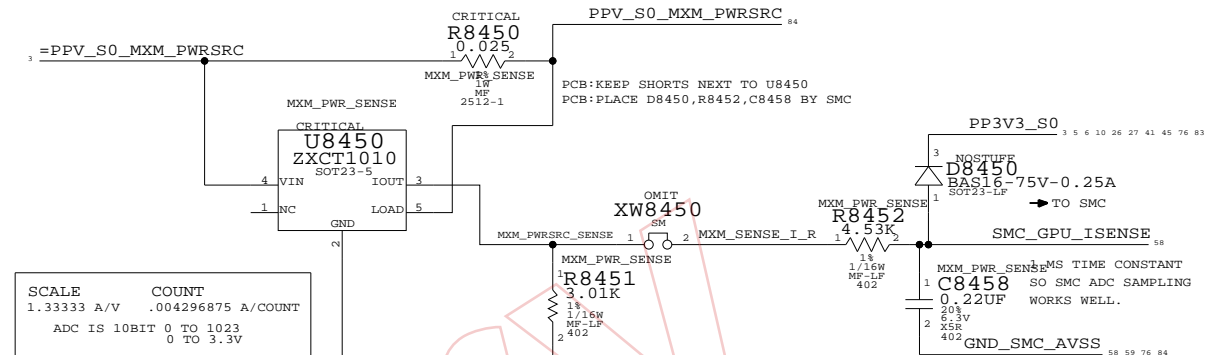
M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

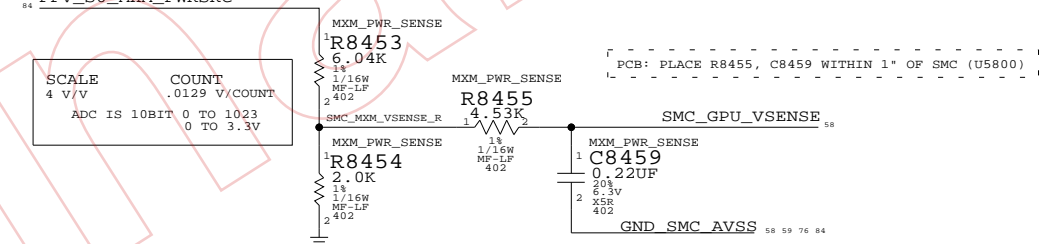
PLACE CAPS NEAR NB

13 s	PEG R2D C P<0>	C8420	0.1uF	1	2	5	PEG R2D P<15>	40	PEX_TX15_L	37	PEG D2R P<0>	6 13
13 s	PEG R2D C N<0>	C8421	0.1uF	1	2	5	PEG R2D N<15>	42	PEX_TX15	39	PEG D2R N<0>	6 13
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13 s	PEG R2D C N<1>	C8423	0.1uF	1	2	5	PEG R2D N<14>	46	PEX_TX14_L	43	PEG D2R N<1>	6 13
13 s	PEG R2D C P<2>	C8424	0.1uF	1	2	5	PEG R2D P<13>	48	PEX_TX14	45	PEG D2R P<2>	6 13
13 s	PEG R2D C N<2>	C8425	0.1uF	1	2	5	PEG R2D N<13>	50	GND24	47	PEG D2R N<2>	6 13
13 s	PEG R2D C P<3>	C8426	0.1uF	1	2	5	PEG R2D P<12>	52	PEX_TX13_L	49	PEG D2R P<3>	6 13
13 s	PEG R2D C N<3>	C8427	0.1uF	1	2	5	PEG R2D N<12>	54	PEX_TX13	51	PEG D2R N<3>	6 13
13 s	PEG R2D C P<4>	C8428	0.1uF	1	2	5	PEG R2D P<11>	56	GND25	53	PEG D2R P<4>	6 13
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13 s	PEG R2D C N<15>	C8451	0.1uF	1	2	5	PEG R2D N<0>	102	PEX_TX5	99	PEG D2R N<15>	6 13

MXM PWRSRC (GPU CORE) CURRENT SENSE



MXM PWRSRC VOLTAGE SENSE (SCALING 12V INPUT VOLTAGE TO SMC)



MXM PCI-E & PWR

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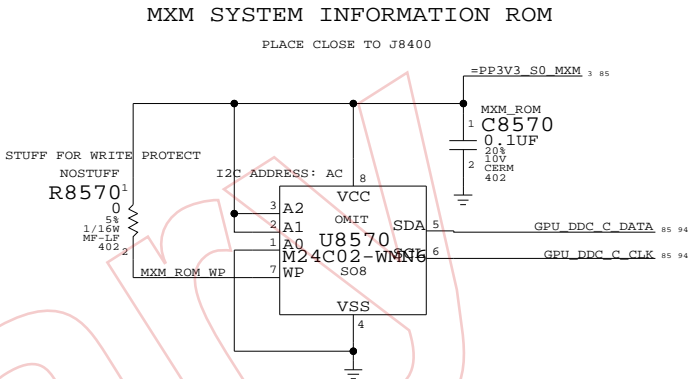
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE	SHT	84 OF 97
NONE		

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Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)
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MXM SPEC POWER REQUIREMENTS (NOT NECESSARILY THE SAME FOR EVERY MODULE)		
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

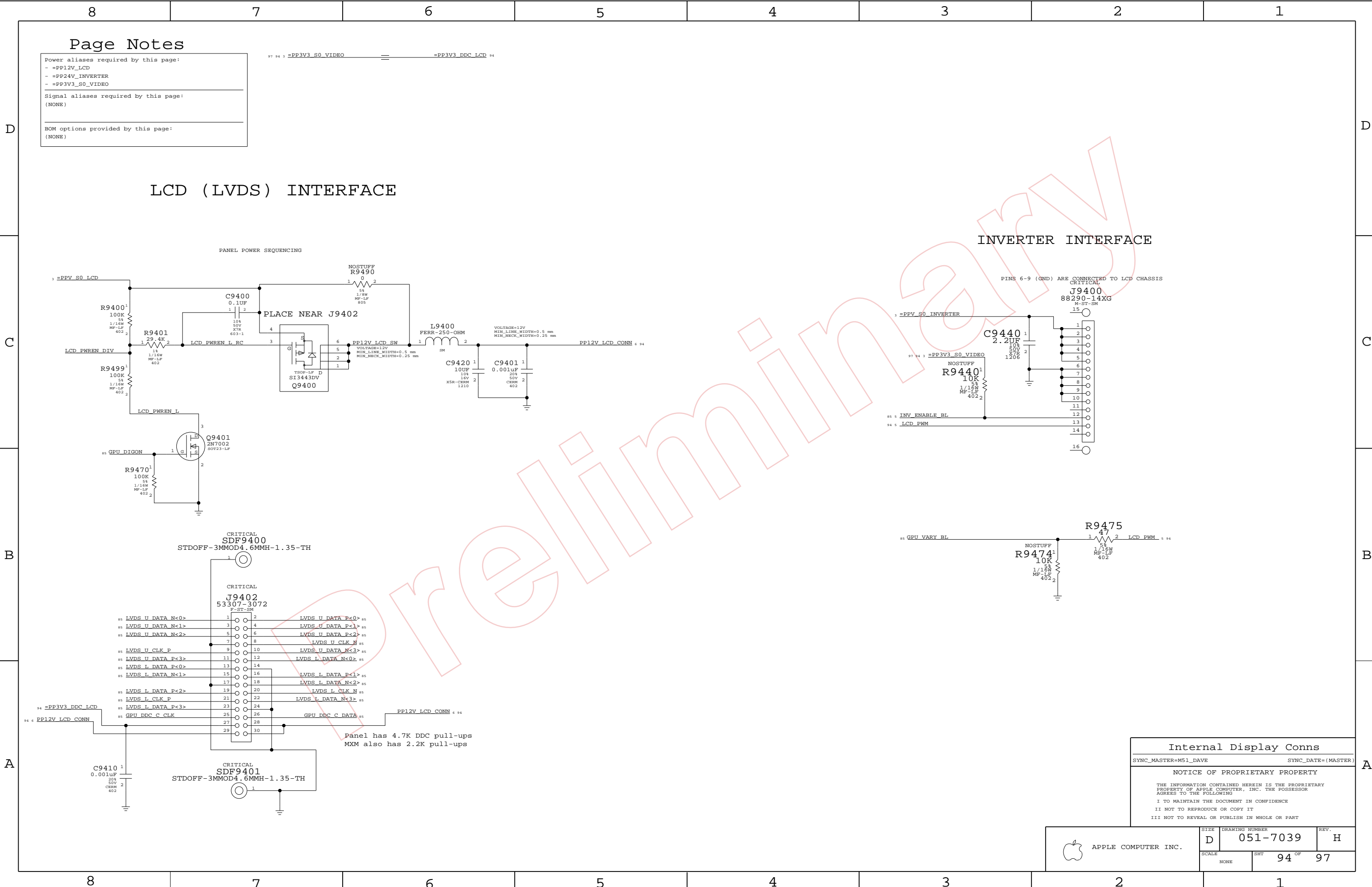


MXM I/O	
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SIZE D	DRAWING NUMBER 051-7039	REV. H
SCALE NONE	SHT 85	OF 97



Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

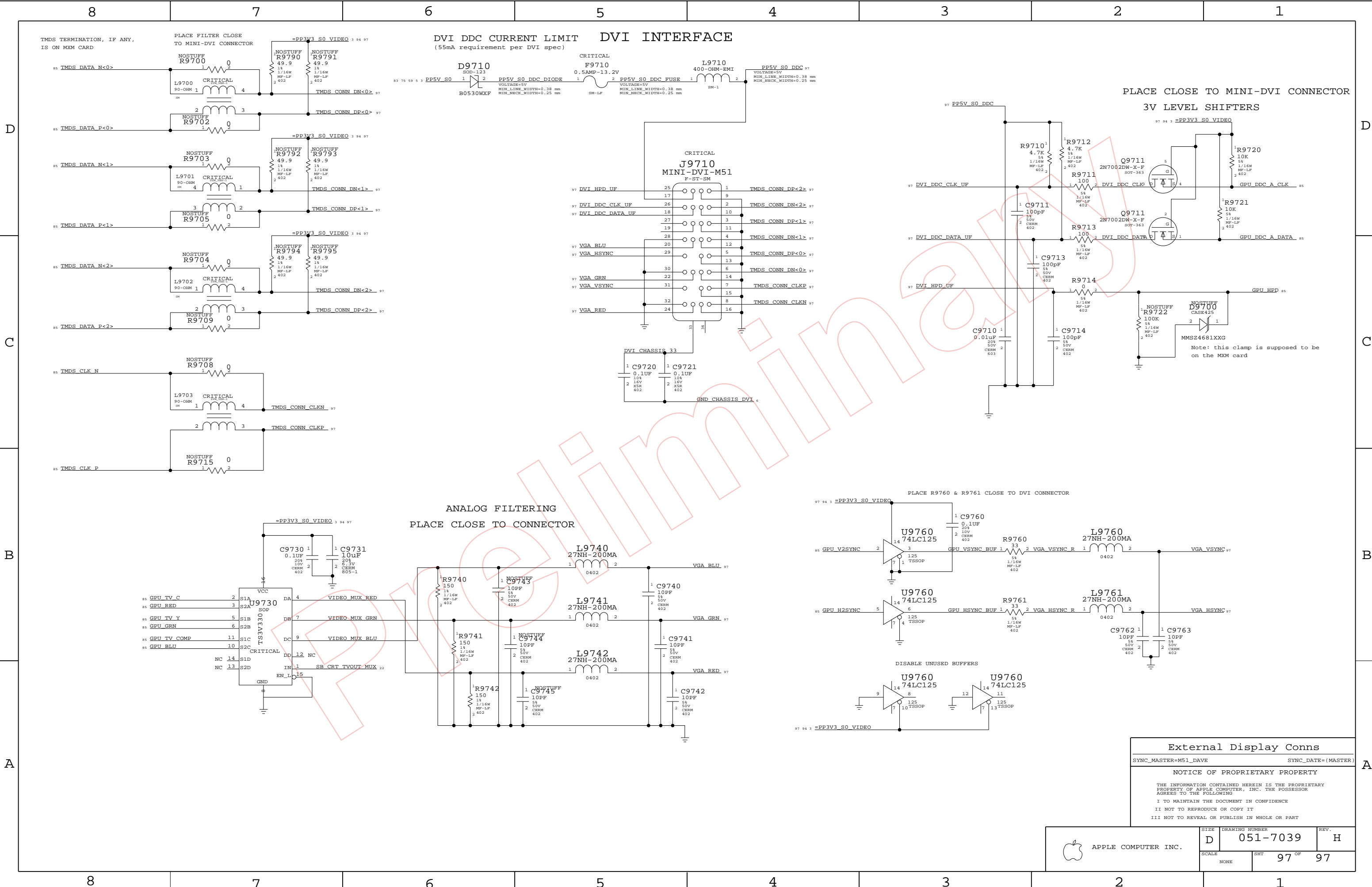
Signal aliases required by this page:
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BOM options provided by this page:
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LCD (LVDS) INTERFACE

INVERTER INTERFACE

Internal Display Conns		
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External Display Conns

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